M/E/TX

Reg. No: 22BIT0037

Final Assessment Test – May 2024

VIT® Vellore Institute of Technology

Course: **BITE301L - Computer Architecture and Organization**

Class NBR(s): **3712/3720/3765**

Slot: **C1+TC1**

Time: **Three Hours**

Max. Marks: **100**

- **KEEPING MOBILE PHONE/ELECTRONIC DEVICES EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

Answer any TEN Questions

(10 X 10 = 100 Marks)

1. a) Write an Assembly Language Program using assembly notations for implementing the expression **[5]**

X=(A-B)/(C+D)

Consider that the data values are stored in memory location starting from 500 onwards and the program is stored from memory location 250 onwards.

b) Given the following memory values and a one-address machine with an accumulator. What values do the following instructions load into the accumulator? Consider that the instruction is stored in address 200. **[5]**

i) LOAD IMMEDIATE 50
ii) LOAD DIRECT 50
iii) LOAD INDIRECT 50
iv) LOAD RELATIVE 20
v) LOAD REGISTER INDIRECT

Memory Address	Data
23	12
50	23
220	67
221	87
300	45

PC	200
R0	300

2. Compute Memory Traffic, total memory for encoding and storing code for 3,2,1,0 address machines that implements the expression evaluation A=(B-C)*D. Assume that the opcode occupies one byte, addresses occupy two bytes, data values also occupy two bytes and 1 byte word length.

Template: (Follow for all types)

3-addr Instruction

Instruction	Memory to Store	Memory to Encode	M/A's to Fetch	M/A's to Execute	Total Memory Traffic
				Total	

3. Show step by step multiplication process using Booth Algorithm when the following numbers are multiplied. Assume eight bit registers that hold signed numbers. (Use the following template)

(-14) * (+39)

A	Q	Q_{n+1}	Operation/ Action	Count/Iteration Number

4. A computer employs RAM chips of 512 * 16 and ROM chips of 1024 * 8. Design the memory system with memory mapped I/O which needs 1K * 16 of RAM, 2K * 16 of ROM and 1 interface unit with 512 registers each.

5. a) Design the following set of instructions using a 5 stage instruction pipeline. If any hazards occur, identify those hazards and redesign the pipeline for rectifying each hazard. **[6]**

ADD R3,R1,R2

SUB R3,R2,R1

NAND R4, R3, R1

OR R0,R3,R4

XOR R1,R4,R3

F D E M W

b) Calculate the time taken (for the above set of instructions) by the pipelined processor with and without hazard if each instruction takes a cycle time of 10 ns and the time is evenly distributed among the stages. Compare the throughput of this pipelined processor with the unpipelined processor. Assume that there is no latency delay in the pipeline system. **[4]**

6. Compare and contrast program controlled I/O and Interrupt Initiated I/O with proper illustrations.

7. Illustrate the different types of interconnection networks in multiprocessor systems with examples.

8. a) A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. **[5]**

i) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.

ii) Calculate the format of memory address if the cache is organized as a 2-way set-associative cache.

b) Consider a computer system with a memory hierarchy consisting of logical and physical addresses. The logical address space of the system is 32 gigabytes (GB), and the physical address space is 16 megabytes (MB). The page size is 4 kilobytes (KB), page entry size (8 Bytes). Determine the number of pages, the number of frames, and the size of the page table for this system. **[5]**

9. Show step by step division process using Restoring Division Algorithm when the following numbers are divided. (Use the following template)

(-94) / (+3)

A	Q	Operation/ Action	Count/Iteration Number

10. a) Assume that you have a byte-addressable machine that uses 32-bit integers and you are storing the hex value 1234 at address 0: **[4]**

i) Show how this is stored on a big endian machine.

ii) Show how this is stored on a little endian machine.

Address	00	01	10	11
BigEndian				
Little Endian				

b) If computer A has clock rate of 3.2 GHz and requires 10s to run program X, we need to design a computer B which executes the same program X with the following attributes: CPU time is 8s and clock cycles = 1.4*clock cycles of A. What is the clock rate of computer B? [3]

c) Suppose a cache is 10 times faster than main memory and suppose cache can be used 90% of the time, how much speedup do we gain by using the cache? [3]

11. a) Design the following set of instructions using a 5 stage instruction pipeline. If any hazards occur, identify those hazards and redesign the pipeline for rectifying each hazard. [5]

I0: ADD R4 = R1 + R0;

I1: SUB R9 = R3 - R4;

I2: LDW R2 = MEM[R3 + 100];

I3: STW MEM[R4 + 100] = R2;

Where R1, R0, R3 and R4 are operands for ADD and SUB, LDW is for loading data in register, STW is for storing data in memory.

b) Calculate the time taken (for the above set of instructions) by the pipelined processor with and without hazard if each instruction takes a cycle time of 15 ns and the time is evenly distributed among the stages. Compare the throughput of this pipelined processor with the unpipelined processor. Assume that there is a latency delay of 5ns in the pipeline system. Use the following template for comparing the performance. [5]

Time taken in Unpipelined	**Time taken in Pipelined (Without Hazard)**	**Time Taken in Pipelined (With Hazard Rectification)**

If the throughput has to be increased still further, calculate the maximum increase that could be achieved.

12. a) Represent the following decimal number in IEEE 754 32 bit and 64 bit floating point notation $(263.3)_{10}$ [5]

b) When an arithmetic instruction is executed the execution time is [5]

- 4 clock cycles if the operands can be fetched from the cache (cache hit)
- 14 clock cycles if the operands have to be fetched from main memory (cache miss).

The cache hit ratio is 0.6, i.e., 60% of the time the required operands are in the cache. How many clock cycles are needed on average to execute the instruction?

⇔⇔⇔ M/E/TX⇔⇔⇔