Final Assessment Test – November 2024

VIT
Vellore Institute of Technology

Course: **BECE102L - Digital Systems Design**

Class NBR(s): **4253 / 4259 / 4263 / 4265 / 4267 / 4270 / 4272 / 4275 / 4277 / 4279 / 4282 / 4285 / 4290 / 4291 / 4294 / 4298 / 4300 / 4302 / 4306**

Slot: **E2+TE2**

Time: **Three Hours**

Max. Marks: **100**

- **KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Simplify the following using De-Morgan's theorem and draw the circuit using CMOS logic.

$$\overline{\overline{a + b\bar{c} + d(e + \bar{f})}}$$

2. a) Simplify the following to SOP using K – Map.

Y (A, B, C, D) = ∑m(0,1,3,7,9,15) + d(2,4,10, 13) and draw the circuit diagram using basic gates.

b) Realise the simplified function from (2(a)) using only NOR gates.

3. Find the result of the following expression

a) X = 4'b1010; Y = 4'b1101; Z = 4'b10x1

i. ~X

ii. X ^ Y

iii. (X ^~ Y)&& Z

b) reg A; reg [1:0]B, C; reg [2:0]D;

A = 1'b1; B = 2'b00; C = 2'b10; D = 3'b110;

i. Y ={ 4{A} , 2{B} , C }

ii. Y = {3{A}, 3{B[1]}, 2{D[2]}}

4. **Scenario**: Design a simple home automation system that controls the lights based on different conditions.

Inputs:

- **A**: Light Switch (1 if switched ON, 0 if OFF)
- **B**: Motion Sensor (1 if motion detected, 0 otherwise)
- **C**: Day/Night Sensor (1 if it is night, 0 if it is day)

Tasks:

i. **Develop a truth table** for when the lights should be ON based on the given conditions:

   a. Lights ON if the switch is ON.

   b. Lights ON if motion is detected at night.

ii. **Derive the logic expressions** for the light control based on the truth table.

iii. **Implement the logic expressions** using basic gates and provide the circuit diagram.

iv. Write the Dataflow HDL.

5.(a) A combinational logic circuit has four inputs (A, B, C, and D) and one output Z. The output is 1 if the input has three consecutive 0's or three consecutive 1's. For example, if A = 1, B = 0, C = 0, and D = 0, then Z = 1, but if A = 0, B = 1, C = 0, and D = 0, then Z = 0. Design using 4:1 MUX considers B & D as Selection Lines.

OR

5.(b) Implement the following Boolean function $F(A, B, C, D) = \Sigma m(1, 2, 4, 6, 7, 8, 12, 15)$ using 3:8 Decoder and external gates.

6. A half adder is a circuit that adds two bits to give a sum and a carry. Give the truth table for a half adder, and design the circuit using only two gates. Then design a circuit which will find the 2's complement of a 4-bit binary number. Use half adders and any additional gates.

7. Design the right-shift register circuit using four D flip-flops with clock enable, four 2-to-1 MUX, and a single OR gate.

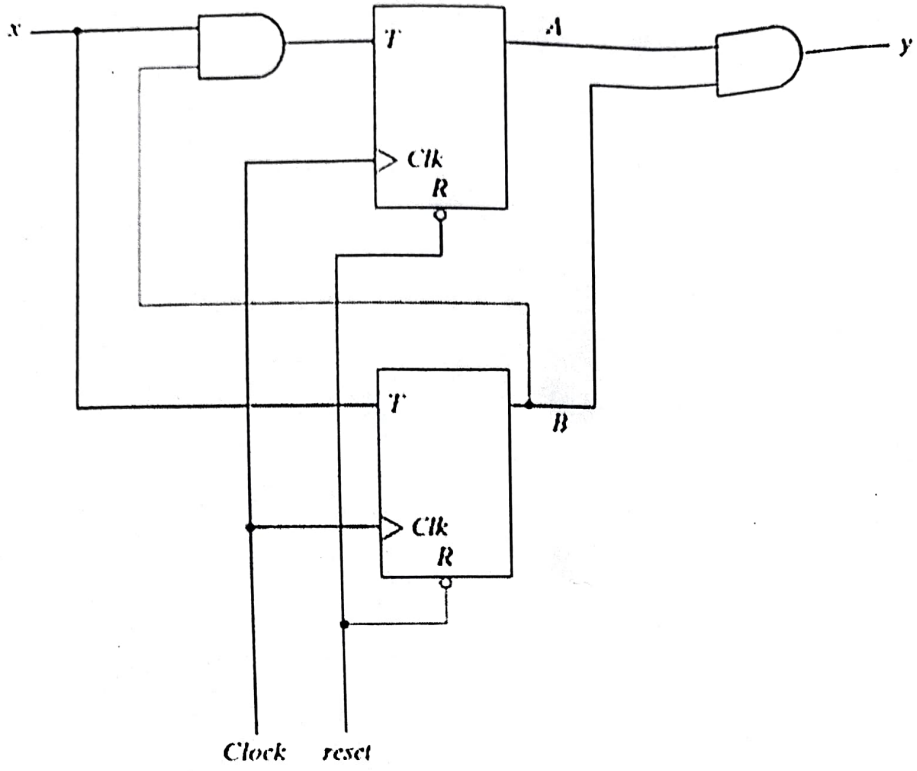
8. Design a counter for the given sequence using JK – FF. Write behavioural Verilog code for the design.

   0→2→3→ 7→ 8→11→15→0...

9.(a) Design a Mealy Sequential Circuit whose output is 1, whenever the input sequence ends with 0011.

OR

9.(b) Analyse the given circuit and draw the state diagram and state table.



10. Design the following using PLA to satisfy the following Boolean algebra

F1 = AC' + B'C

F2 = B'C + A'B'C' + ABC

⇔⇔⇔ F/L/TX⇔⇔⇔