

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2024-2025

REG.NO.:

SLOT: E2+TE2

Programme Name & Branch : B.Tech/ BCI, BCB, BCE, BCT, BDS, BKT, BAI
Course Code and Course Name : BECE102L/ Digital Systems Design
Faculty Name(s) : ANITHA R, PRIYADHARSHINI B, LAVANYA N, PALLA
PENCHALAI AH, AVINASH CHANDRA, RAJESH N, SHWETA B THOMAS, NAVEEN MISHRA, SAURABH
NAGAR, ANJU THOMAS, SIDHARTH GAUTAM, JAFFINO, HEMANTA KUMAR SAHU, NAWAZ SHAFI,
VETRIVEERAN RAJAMANI, GEORGE JACOB, SWATI G, ASHUTOSH MAHAJAN, NISHA J S
Class Number(s) : VL2024250104302, VL2024250104259, VL2024250104253, VL2024250104265,
VL2024250104270, VL2024250104279, VL2024250104306, VL2024250104275, VL2024250104294, VL2024250104290,
VL2024250104272, VL2024250104267, VL2024250104263, VL2024250104277, VL2024250104291, VL2024250104285,
VL2024250104298, VL2024250104300
Date of Examination : 17-Oct-2024
Exam Duration : 90 minutes
Maximum Marks: 50

General instruction(s):

- Answer All Questions

Questions

1. Draw the hardware logic that get inferences for the following code, draw the truth table. Write the test bench to verify the functionality. 10
- ```
module cat2q1 (in1, out1, out2);
 input [2:0]in1;output out1, out2;
 reg temp;
 always@(in1)
 begin
 temp <= in1[0]^in1[1]^in1[2];
 if(temp)
 begin
 out1 <= 1'b1;
 out2 <= 1'b0;
 end
 else
 begin
 out1 <= 1'b0;
 out2 <= 1'b1;
 end
 end
 end
endmodule
```
2. Using a flowchart, demonstrate the multiplication of 5 and -13 using the booth algorithm. 10
- Assume 5 and -13 of 5 bits.
3. Design a 2 bit comparator and use it to construct a 4 bit comparator. 10



SCHOOL OF ELECTRONICS ENGINEERING  
CONTINUOUS ASSESSMENT TEST - II  
FALL SEMESTER 2024-2025

REG.NO.:

SLOT: E2+TE2

4. Consider a certain type of flip-flop with inputs  $X_1$  and  $X_2$  and excitation table as:

10

| Present State | Next State | Inputs |       |
|---------------|------------|--------|-------|
|               |            | $X_1$  | $X_2$ |
| $Q_n$         | $Q_{n+1}$  |        |       |
| 0             | 0          | 0      | 0     |
| 0             | 1          | 0      | 1     |
| 1             | 0          | 0      | X     |
| 1             | 1          | 1      | X     |

Design a synchronous counter using this flip-flop for the count sequence 0, 1, 3, 5, 6, 0, by considering that if the present state is an undesired one, it should transit to 0 on application of clock pulse.

5. A sequential circuit has two JK flip-flops with outputs  $Q_A$  and  $Q_B$  and one input  $x$ . The circuit is described by the following flip-flop input equations:  $J_A = x$ ,  $K_A = Q_B$ ,  $J_B = x$ ,  $K_B = \overline{Q_A}$ .

(a) Derive the state equations  $Q_A(t+1)$  and  $Q_B(t+1)$  by substituting the input equations for the J and K variables. (b) Draw the state diagram of the circuit.

\*\*\*\*\*