S/K/TY

Reg. No: 24BB[redacted]

VIT
Vellore Institute of Technology

Final Assessment Test – November 2025

Course: **CBS1004** - **Computer Architecture and Organization**

Class NBR(s): **3255** Slot: **B1**

Time: **Three Hours** Max. Marks: **100**

- **KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

COs	CO Statements
CO1	Provide fundamentals on machine instructions and addressing modes.
CO2	Comprehend the various algorithms for computer arithmetic.
CO3	Analyse the performance of various memory modules in memory hierarchy.
CO4	Compare and contrast the features of RAID architectures of organization and structure of disk drives.
CO5	Outline the evaluation of multicore architectures.

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions

(10 X 10 = 100 Marks)

1.	a)	Provide the memory specification and register configuration of the IAS computer and describe its instruction format.	[6]	CO1	BL1
	b)	Write an IAS assembly language program to evaluate the arithmetic expression: $O = \big(A \times (B - C)\big)$. Assume that A, B, C are at locations 500, 501, 502. Store the result at 400.	[4]		
2.	a)	State various addressing modes with suitable examples.	[6]	CO1	BL1
	b)	An instruction is stored at location 400 with its address field at location 401. The address field has the value 600. A processor register R1 contains the number 100. Evaluate the effective address if the addressing mode of the instruction is: i. Direct ii. Indexed with R1 as the index register.	[4]		
3.	a)	Define the principle of pipelining and state its objectives.	[3]	CO1	BL3
	b)	Give various elements of data path and draw a sketch of single bus data path.	[3]		
	c)	A four-stage pipeline has stage delays of 150 ns, 120 ns, 160 ns, and 140 ns, respectively. Pipeline registers are placed between the stages, and each register introduces a delay of 5 ns. Assuming a constant clock rate (determined by the slowest pipeline stage plus register delay), what is the total time required to process 1000 data items on this pipeline?	[4]		
4.	a)	Explain in detail the differences between RISC and CISC architectures.	[4]	CO1	BL3
	b)	Illustrate the operation of a hardwired control unit with a neat sketch.	[6]		

5.	Consider a multiplier circuit that uses the Booth algorithm to multiply two signed numbers: +17 (multiplicand) and -10 (multiplier), represented in two's complement form. Perform the Booth recoding of the multiplier, compute the product step by step using the Booth algorithm.		CO2	BL3
6.	a) The dividend 17 is stored in register Q and the divisor 5 in M register. Perform the division using restoring division. b) Perform 2's complement subtraction of the minuend 17 and subtrahend 32 using 8 bit ALU and give the status of overflow flag.	[7] [3]	CO2	BL2
7.	Describe the characteristics and working of magnetic disk storage. Illustrate your answer with a labeled structural diagram of a disk drive.		CO4	BL2
8.	a) Explain Flynn's taxonomy of computer architectures with diagrams. Give examples for each category. b) Compare single-core and multi-processor systems in terms of performance, cost, power consumption and scalability.	[6] [4]	CO5	BL4
9.a)	Consider a cache memory with a capacity of 1024 MB and a block size of 256 bytes. The main memory size is 256 GB. Determine how the physical address is divided for the following mapping techniques: i. Direct mapping. ii. Fully associative mapping. iii. 4-way set associative mapping.	 [3] [3] [4]	CO3	BL3
	OR			
9.b)	A computer system uses RAM chips of 256 × 8 and ROM chips of 128 × 8. You are required to design a system that includes 512 × 16 of RAM, 256 × 8 of ROM, and two interface units, each containing 256 registers. The system has an address bus width of 16 bits and a data bus width of 16 bits. A memory-mapped I/O configuration is used, and the two most significant bits of the address bus are assigned as follows: • 00 → RAM • 01 → ROM • 10 → Interface registers i. Determine the total number of chips required for the design. ii. Develop the memory interface address map for the system. iii. Illustrate the chip layout for the given design.		CO3	BL3
10.a)	i. Compare I/O-mapped I/O and memory-mapped I/O, highlighting their respective advantages and disadvantages. ii. Explain how communication between an I/O device and the processor is established using strobe and handshaking techniques. Also, discuss the need for a buffering mechanism.	[4] [6]	CO3	BL2
	OR			
10.b)	Assume you are designing a control unit to enable direct data transfer between an I/O device and the main memory without requiring constant processor involvement. Explain the function and significance of the DMA controller in this system.		CO3	BL2

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