VIT

Vellore Institute of Technology

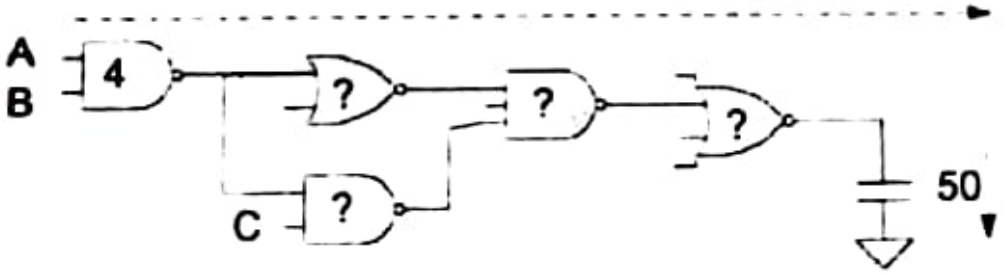
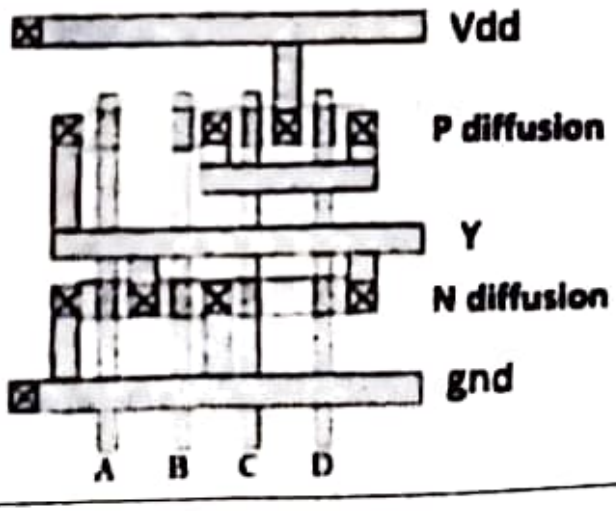
SCHOOL OF ELECTRONICS ENGINEERING (SENSE)

Discipline : B.Tech
Subject : VLSI System Design
Max. Marks : 50
Class number: VL2023240503816

Course code : BECE303L
Slot: A1
Time : 90 min
Semester: Winter 2023-24

CAT-II

Answer ALL Questions

S.No	Question	Marks	CO	BL
1.	Draw the schematic of Y = (A+B.C+D.E.F)' in static CMOS with sizing such that the pullup and pull down path resistance of the circuit is equal to pullup and pull down path resistance of the unit sized CMOS inverter. Assume resistance of the PMOS is twice of resistance of NMOS resistor. Evaluate the rising delay and falling delay of worst case path delay.	10	3	BL4
2.	Estimate the minimum delay of the path which is shown in dotted line and choose transistor sizes to achieve this delay. 	10	3	BL4
3.	Identify the output expression of the following layout. 	10	4	BL5

4	Draw the stick diagram for the following function and estimate the area. $Z = (A + B + (C . (D + E)))'$	10	4	BL4
5	a) Sketch the schematic of 2 input XNOR gate in Cascode Voltage switch logic b) Sketch the schematic of $Z = (A + (B + C) . (D + E))'$ in Pseudo- NMOS logic	10	5	BL5