VIT
Vellore Institute of Technology

Final Assessment Test – November 2022

Course: BECE102L - Digital Systems Design

Class NBR(s): 2859 / 2862 / 2864 / 2866 / 2869 / 2871 / 2873 / 2875 / 2877

Slot: F1+TF1

Time: Three Hours

Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS TREATED AS EXAM MALPRACTICE

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Write the Boolean equation for the circuits of Fig.1. Use De Morgan's theorem and Boolean algebra rules to simplify the equation. Draw the simplified circuit using only NAND gates.

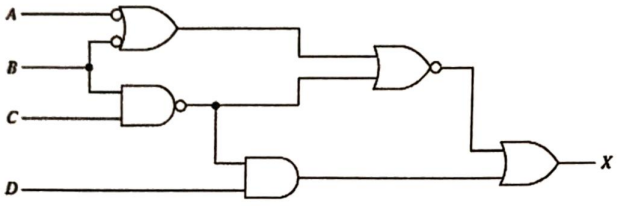


Fig. 1

2. Simplify the following Boolean expression using K- Map and implement the circuit diagram using only NOR gates.

$$F = \bar{B}\bar{C} + A\bar{B} + AB\bar{C} + A\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}CD$$

3. Develop 3-bit input(x, y and z) XOR gate in Verilog HDL using AND, OR and NOT gates primitives. Write the truth table, derive the expression and Write the stimulus (test bench) mode that exercises all combinations of x, y and z.

4. Implement the function

$$F = \overline{W_1}\,\overline{W_2}\,\overline{W_3}\,\overline{W_4} + W_1W_2 + W_1W_3 + W_1W_4 + W_3W_2W_4$$

by using only one 4-to-1 multiplexer with W_2 and W_4 as the selection lines and using external gates. And also write the Verilog HDL gate level for the design.

5. The circuit has 3-bit binary inputs (A_2,A_1,A_0) and their 2's complement as output (D_2,D_1,D_0) write its truth table and then design using full adder.

6. (a) Design a block diagram of a 4-bit increment/decrement circuit using 1-bit increment/decrement circuit controlled by an i_d signal (increment when i_d = 1, decrement otherwise).

OR

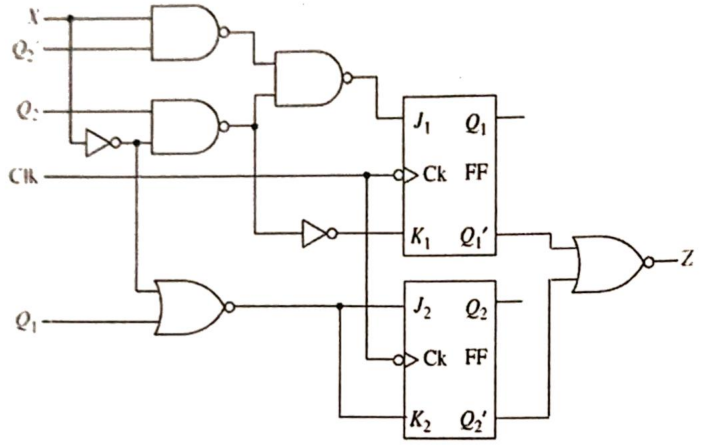
6. (b) Design a 4–bit magnitude comparator using 2-bit magnitude comparators.

7. Consider the circuit shown below.

(a) Construct a state table and state diagram. Is the circuit a Mealy or Moore circuit? Does the circuit have any unused states? Assume 00 as the initial state.

(b) Draw a timing diagram for the input sequence $X = 01100$.

(c) What is the output sequence for the input sequence given in (b)?

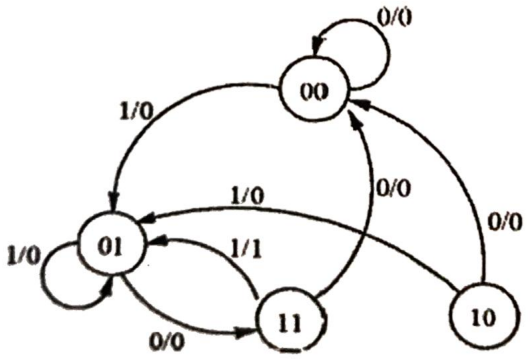


8. Design a synchronous counter using D flip-flops for the given sequence

4 → 2 → 5 → 1 → 7 → 4.....

Write a D-FF using behavioural modelling Verilog HDL and counter using structural modelling.

9. (a) Consider the following state diagram for a circuit with one input X and one output Z. Analyse this state diagram and draw its circuit implementation using JK flip-flop (state Q0) and T flip-flop (state Q1) and MUX-4x1 for Z.



OR

9. **(b) Design a Mealy Sequential Circuit whose output is 1, whenever the input sequence ends with 1001. Design a circuit using T flip-flop.**

10. **Design a BCD to Gray code converter and realize using PAL.**