VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.: 24BCE3000

SLOT: A1+TA1

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2025-2026

Programme Name & Branch	**: BCE, BAI, BCB, BCI, BCT, BCT, BDS, BKT, BME, BEL, BYB**
Course Code and Course Name:	**BCSE205L and Computer Architecture and Organization**
Faculty Name(s)	**: Common to all classes**
Class Number(s)	**:VL2025260501998, 1988, 1903, 2001, 1866, 1985, 1870, 1953, 1898, 4005, 1901, 2024, 5391, 1880, 3865, 1896, 2022, 2006, 1968, 1873**
Date of Examination	**: 15/03/2026**
Exam Duration	**: 90 minutes**

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:

  CO1: Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating-point arithmetic operations.

  CO2: Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements.

  CO3: Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.

Q. No	Question	M	CO	BL
1.	A) Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1000 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D. (i) Find the clock cycles required in both cases. (ii) Which implementation is faster and how much?	7	CO1	BL3
	B) Assume that for a given program 70% of the executed instructions are arithmetic, 10% are load/store, and 20% are branch. Given this instruction mix and the assumption that an arithmetic instruction requires 2 cycles, a load/store instruction takes 6 cycles, and a branch instruction takes 3 cycles, find the average CPI.	3		

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2.	A computer system employs RAM chips of 512 MB each and ROM chips of 256 MB each. The system requires 1 GB of RAM, 512 MB of ROM, and two interface units of 512MB each. Design the memory chip layout for the above requirements. Also determine the number of RAM and ROM chips required and explain the address decoding scheme. i. How many RAM and ROM chips are needed? ii. Draw a memory-address map for the system. iii. Give the address range in hexadecimal for RAM, ROM, and interface. iv. Show the chip layout for the above design	10	CO2	BL3
3.	A computer system has a 4-way set associative cache with a capacity of 256 bytes. Each cache block contains one word (4 bytes). The sequence of byte addresses referenced by the processor is: 8, 64, 96, 128, 64, 96, 256, 192, 24 Assume that the cache is initially empty and the replacement policy is LRU (Least Recently Used). i. Determine the block address and set number for each reference. ii. Construct a cache simulation table for the given memory references, indicating hit or miss for each reference. Also show the final cache contents and the total number of hits and misses.	10	CO2	BL3
4.	A) The following memory addresses are given: 000101, 000110, 000111, 001000 A memory system has 4 memory modules, each with 16 locations. The processor generates 6-bit addresses. Divide the 6-bit address into module bits and location bits for High-Order and Low-Order Memory Interleaving, and determine the module and location for the given addresses while showing how consecutive addresses are distributed among the modules. B) A system uses Interrupt-driven I/O to transfer data from an input device. The device generates one interrupt for every 8 bytes transferred. If the device transfers 256 bytes, determine: i. The total number of interrupts generated. ii. Explain how interrupt-driven I/O improves CPU utilization compared to programmed I/O.	6 4	CO3	BL2
5	A) A system uses DMA to transfer a 32 KB block of data from an I/O device to main memory at a rate of 40 MB/s. The processor runs at 400 MHz and spends 400 clock cycles to initiate the DMA transfer and 800 clock cycles to complete it after the transfer finishes. Determine the percentage of processor time consumed during the DMA transfer. B) A high-speed printer is connected to a computer system. The printer is slower than the CPU, causing delays in data transfer. Explain how buffering can be used to improve data transfer between the CPU and the printer. Illustrate the concept with a simple diagram.	5 5	CO3	BL3

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