Final Assessment Test – November/December 2023

VIT
Vellore Institute of Technology

Course: BECE102L - Digital Systems Design

Class NBR(s): 4154 / 4156 / 4157 / 4159 / 4160 / 4162 / 4164 / 4165 / 4166 / 4167 / 4169 / 4171 / 4173 / 4174 / 4175 / 4176 / 4178 / 4179 / 4183 / 4187 / 4255 / 4259 / 4263 / 4267 / 4288

Slot: B2+TB2

Time: Three Hours

Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN "OFF" POSITION, IS TREATED AS EXAM MALPRACTICE

General Instructions :

1. **Assume suitable values, in case of any missing data.**
2. **Necessary intermediate steps for each solution is mandatory**

Answer ALL Questions

(10 X 10 = 100 Marks)

1. A circuit has three inputs (A2, A1, A0) and one output (Y). The inputs (A2, A1, A0) represent a number from 0 to 7. Output Y is true if the number is prime.
   a) Write the truth table.
   b) Write the function in canonical sum-of-products form.
   c) Write the function in canonical product-of-sums form.
   d) Identify the simplified expression using Boolean algebra and draw the CMOS circuit diagram for the simplified expression.

2. Minimize the following expression using K-map to identify the minimum SOP and POS expressions. Implement the minimal SOP and POS expressions using NAND gates respectively.
   a) $F(A,B,C,D) = \Sigma m(1,4,5,6,12,14,15)$
   b) $F(A,B,C,D) = \Sigma m(2,3,6,7,12,13,14)$

3. Implement the minimized form of given Boolean function using gate level modelling in Verilog HDL. Also write the testbench to verify the design.

   $F(A,B,C,D)=A'B'C'D'+A'BC'D+AB'CD'+ABCD$

4. Design a combinational circuit with three inputs, x, y and z and three outputs, A, B and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input. Model the functionality of this combinational circuit using data flow modelling.

5. Design a 4 to 2 priority encoder considering i1 as highest priority and i3 as lowest priority. (i1>i2>i0>i3).

6. Write the Algorithm of booth's multiplier considering multiplicand as -14 and multiplier as 9. Also draw sample block diagram architecture proposed for the above operation.

7. Consider JK flip flop as a given flip flop-

a) Write characteristics table and characteristic equation.

b) Write excitation table and input equations.

c) Write a verilog code for the design using structural modelling.

d) Implement the JK flip flop using SR flip flop.

8. Design a synchronous counter using T-FF for the following sequence -0-3-5-7-9-11-13-15-0.

9. Design a finite overlapped Moore state machine (FSM) for a prime number 010 detector. You need to provide the state transition table and the state transition diagram. Assume that the state is stored in three D-FFs.

10. Implement the following two Boolean functions with a PLA and PAL:

$$F1(A, B, C) = \sum(0, 1, 2, 4)$$

$$F2(A, B, C) = \sum(0, 5, 6, 7)$$

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