VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT: A2

School of Computer Science Engineering and Information Systems

CONTINUOUS ASSESSMENT TEST - I

WINTER SEMESTER 2024-2025

Programme Name & Branch	**: B.Tech (IT)**
Course Code and Course Name	**: Computer Architecture and Organization & BITE301L**
Faculty Name(s)	**: Dr. Vanitha M, Dr. Angulakshmi M, Dr. Meenatchi S**
Class Number(s)	**: VL2024250502719, VL2024250502704, VL2024250502725**
Date of Examination	**: 27.1.25**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes

[CO1-Elucidate the arithmetic operations, addressing modes and the performance of computers
CO3-Analyse the arithmetic algorithms to perform ALU operations]

Q.No.	Question	M	CO	BL
1.	(a) List the steps needed to execute the machine instruction: **Load R2, LOC** in terms of transfers between the components of processor. Assume that the address of the memory location containing this instruction is initially in register PC. (b) Analyse the status of the condition code flags when the following instruction is executed. Add R1, R2 where **$R1=(EE)_{16}$, $R2=(DF)_{16}$**	6 4	CO1	BL2
2.	(a) Program execution time T is to be examined for a certain high-level language program. The program can be run on a RISC or a CISC computer. Both computers use pipelined instruction execution, but pipelining in the RISC machine is more effective than in the CISC machine. Specifically, the effective value of S in the T expression for the RISC machine is 2.1, bit it is only 3.6 for the CISC machine. Both machines have the same clock rate R. (i) What is the largest allowable value for N, the number of instructions executed on the CISC machine, expressed as a percentage of the N value for the RISC machine, if time for execution on the CISC machine is to be longer than on the RISC machine? (ii) Repeat Part (i) if the clock rate R for the RISC machine is 12 percent higher than that for the CISC machine (b) How does program controlled IO works?	6 4	CO1	BL3
3.	(a) Represent the integer 14442 in Big endian and Little endian machine(32-bit). (b)Write an Assembly Language Program to find the average of N numbers using Assembler Directives.	6 4	CO1	BL3

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4.	(a) Define the terms 'stack' and 'subroutine'. How are they useful in implementation of an architecture of a processor (b)Suppose for particular processor Move and Add instructions are available with the formats **Move Location1, Location2** and **Add Location1, Location2** Perform the following operation:Add the contents of memory location A to those of location B, and place the answer in location C.	6 4	CO3	BL2
5.	Assume that an instruction is stored at the location 1000 with its address field at location 1001. The address field has the value 600. The processor register R1 = 900, XR = 200, PC= 400, and BR =700.	10	CO1	BL3

Address	Value
600	700
601	800
602	900
700	950
800	990
899	980
900	1000
901	1050
1000	1150
1100	1200
1300	1700
1500	1800

Write the instruction, to evaluate the effective address and find out the content of AC for the given data if the addressing mode of the instruction is,

a. Immediate addressing mode
b. Direct addressing mode
c. Indirect addressing mode
d. Register addressing mode
e. Register indirect addressing mode
f. Pre and post increment addressing mode
g. Pre and post decrement addressing mode
h. Relative addressing mode
i. Indexed addressing mode
j. Base register addressing mode