



VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO,:

SLOT: C2 + TC2

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch : B.Tech. CSE

Course Code and Course Name : BCSE303L Operating Systems

Faculty Name(s) : Common to all

Class Number(s) : Common to all

Date of Examination : 07/10/2025 (9:30AM – 11:00AM)

Exam Duration : 90 minutes

Maximum Marks: 50

General instruction(s): Answer All Questions

M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyze, 5 – Evaluate, 6 – Create)

Course Outcomes:

CO3. Apply and analyze communication between inter process and synchronization techniques.

CO4. Implement page replacement algorithms, memory management problems and segmentation.

Q. No	Question	M	CO	BL																																																																														
1.	Consider the following snapshot of the system: <table><tr><th rowspan="2">Proce ss</th><th colspan="4">Allocation</th><th colspan="4">Max</th><th colspan="4">Available</th></tr><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>A</th><th>B</th><th>C</th><th>D</th><th>A</th><th>B</th><th>C</th><th>D</th></tr><tr><td>P0</td><td>1</td><td>1</td><td>1</td><td>2</td><td>3</td><td>2</td><td>1</td><td>2</td><td>0</td><td>5</td><td>2</td><td>0</td></tr><tr><td>P1</td><td>1</td><td>0</td><td>2</td><td>0</td><td>1</td><td>6</td><td>5</td><td>0</td><td colspan="4" rowspan="4"></td></tr><tr><td>P2</td><td>1</td><td>3</td><td>4</td><td>4</td><td>2</td><td>3</td><td>5</td><td>6</td></tr><tr><td>P3</td><td>0</td><td>5</td><td>3</td><td>2</td><td>0</td><td>5</td><td>5</td><td>2</td></tr><tr><td>P4</td><td>0</td><td>3</td><td>1</td><td>4</td><td>0</td><td>6</td><td>5</td><td>6</td></tr></table> Using Banker's Algorithm, determine whether the system is in the safe state. (6 Marks) Can a request for <0 3 0 0> from P2 be granted immediately? Justify your answer (4 Marks)	Proce ss	Allocation				Max				Available				A	B	C	D	A	B	C	D	A	B	C	D	P0	1	1	1	2	3	2	1	2	0	5	2	0	P1	1	0	2	0	1	6	5	0					P2	1	3	4	4	2	3	5	6	P3	0	5	3	2	0	5	5	2	P4	0	3	1	4	0	6	5	6	10	2	3
Proce ss	Allocation				Max				Available																																																																									
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P0	1	1	1	2	3	2	1	2	0	5	2	0																																																																						
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P2	1	3	4	4	2	3	5	6																																																																										
P3	0	5	3	2	0	5	5	2																																																																										
P4	0	3	1	4	0	6	5	6																																																																										
2.	The Hardware solution using Test&Set is given below. (instructions are numbered)	10	3	4																																																																														

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Shared variable: boolean waiting[n]; boolean lock;
Initialization: lock = FALSE; waiting[i] = FALSE;
Process i
do
{
11. waiting[i]=TRUE;
12. key=TRUE;
13. While(waiting[i] && key)
    14. key=TestAndSet(&lock);
15. waiting[i]=FALSE;
//CS
16. j=(i+1)%n;
17. while((j!=i)&&!waiting[j])
18.     j=(j+1)%n;
19. If(j==i)
110.    lock=FALSE;
111. else
112.    Waiting[j]=FALSE;
//Remainder section
}while(TRUE);

```

Assume that the following events happen in the given order in a system with four processes(P0-P3)

T1: P0 executes l.1

T2: P0 executes l.2 gets pre-empted

T3: P1 executes l.1

T4: P1 executes l.2

T5: P1 executes l.3 gets pre-empted

T6: P2 executes l.1

T7: P2 executes l.2

T8: P2 executes l.3 gets pre-empted

T9: P3 executes l.1 gets pre-empted

T10: P1 executes l.4 gets pre-empted

Answer the following questions assuming processes get preempted while busy waiting

A) Which process will be the first to enter its critical section and why?

Assume P0 acquires the processor at T11. (3 marks)

B) Which process will the second to enter its critical section and why? (3 marks)

C) Are mutual exclusion and progress implemented in the algorithm? How? (4 marks)

3. a) Assume the following scenario in semaphore solution to the Dining Philosophers synchronization problem (philosophers are seated clockwise)
- Time T0: Philosopher 1 & 2 have executed wait on their left chopstick
- Time T1: Philosopher 0 & 3 have executed wait on their left chopstick
- Time T2: Philosopher 1 has executed wait on right chopstick
- Time T3: Philosopher 3 has executed wait on right chopstick
- Time T4: Philosopher 0 has executed wait on right chopstick
- Time T5: Philosopher 4 has executed wait on right chopstick

5

3 4



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	(i) List the states of the 5 philosophers at time T5. Justify your answer. (2 Marks) (ii) Which philosopher would be the first to eat? (1 Mark) (iii) Give a scenario where philosopher 4 starves. (2 Marks)			
	b) Assume Process "Philosopher 0" is currently in its Critical Section. How does the monitor-based solution to the Dining Philosophers problem ensure that the philosopher 0 properly notifies his hungry neighbours after he finishes eating? Explain the portion of the code that Philosopher 0 executes upon completing his meal.	5		
4.	a) Consider a paging system with a page size of 1 KB, physical memory of 32MB and logical memory of 50,000 Bytes. Each page table entry requires 4 bytes. (i) How many pages are required to represent the logical memory? (ii) How many bits does the physical address contain? (iii) How many bits in the logical address represent the page number? (iv) What is the size of the internal fragment created? (v) What is the size of the page table?	5	4	3
	b) Consider a system with five memory partitions of sizes (in order): 200 KB, 600 KB, 100 KB, 300 KB, 400 KB. Four processes arrive in sequence: P0: 210 KB, P1: 450 KB, P2: 250 KB, P3: 120 KB. Allocate memory for these processes using the following strategies: a. First-Fit b. Best-Fit c. Worst-Fit	5		
5	a) Given four empty frames, how many page faults will occur if the following page replacement algorithms are used on the reference string 7,2,3,4,2,1,5,3,2,1,2,3,7,4,1,2,3,6? (i) FIFO (2 Marks) (ii) LRU (2 Marks) (iii) Optimal (2 Marks)	6	4	3
	b) Calculate the Effective Access Time for a system that suffers from 50%-page fault rate with 100ns for memory access, 1ms for handling page fault overhead, 50ns for restart overhead and 500ns to swap pages in and out.	4		