VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science and Engineering

Winter Semester 2023-2024 Continuous Assessment Test – I

Program Name &Branch: BCB, BCE, BCI, BCT, BDS, BKT **SLOT: D2+TD2**

Course Name & code: Computer Architecture and Organization- BCSE205L

Class Number (s): Common to all

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Answer all five questions

Q.No.	Question	Max Marks
1.	List out the various registers of IAS machine and write the significance of each register. Also demonstrate an assembly code using IAS instructions for the following expression: C=(A+B)/D Assume the inputs are available in the memory locations 101 onwards. Store the result in memory location 104 onwards.	10 [5+5]
2.	a. Draw the flowchart for Booth's algorithm. b. Perform Booth's multiplication for the given numbers -15 and 6 (i.e. -15×6). Description of each step is expected.	10 [4+6]
3.	a. Explain the IEEE 754 floating-point representation. b. Perform the division for the given numbers 21 and 4 (*i.e.* 21/4,) using non-restoring algorithm. Description of each step is expected.	10 [4+6]
4.	a. Discuss the instruction types of IAS machine with suitable example? b. Describe the functional components of a computer with a neat diagram?	10 [5+5]
5.	Write the assembly code for the given arithmetic statement. A= (B+C) *D using 0,1,2 and 3 address instructions and compute memory traffic for 0,1,2 and 3 address machines. Assuming the following fields: addresses - 2 bytes, data values -2 bytes, opcode -8-bits and word length -1 byte.	10 [5+5]