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Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

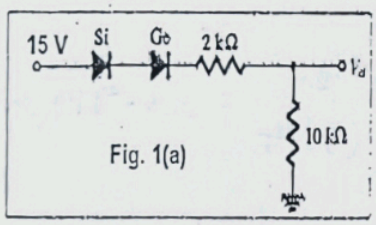
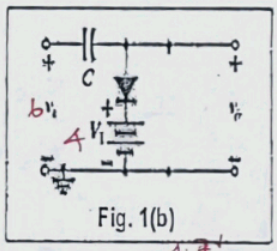
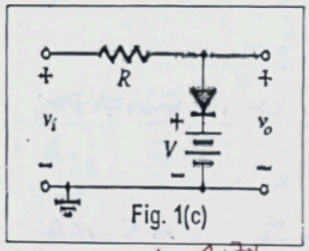
SCHOOL OF ELECTRICAL ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2024-2025

SLOT: C2

Programme Name & Branch	: B.Tech. EEE & EIE
Course Code and Course Name	: BEEE205L - Electronic Devices and Circuits
Faculty Name(s)	: Dr. N. Sudhakar & Dr. G. Arunkumar
Class Number(s)	: VL2025260101212 & VL2025260101213
Date of Examination	: 19-08-2025, Tuesday, 2.00 PM to 3.30 PM
Exam Duration	: 90 minutes Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes **(Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)**
  CO1 – Solve diode circuits for various applications.
  CO2 – Analyze and design BJT and MOSFET DC circuits and their amplifier configurations

Q. No	Question	M	CO	BL
1.	(a) Find the V_O for the multi-diode circuit of Fig. 1(a)	2	1	3
	(b) Sketch the input and output waveforms for the following clamper circuit with a sine wave input of 12 $V_{(p-p)}$, 50 Hz, and a DC battery value of 4 V in Fig. 1(b)	4		
	(c) Sketch the input and output waveforms for the following clipper circuit with a sine wave input of 12 V(p-p), 50 Hz, and a DC battery value of 4 V in Fig. 1(c)	4		
	 Fig. 1(a)  Fig. 1(b)  Fig. 1(c) Fig. 1			
2.	(a) Sketch neatly the PN junction diode forward bias circuit, reverse bias circuit, and plot its Volt-Ampere characteristics curve	5	1	2
	(b) Sketch neatly the half-wave rectifier circuit, and plot its input and output waveforms with input voltage 8 $V_{(p-p)}$. Also, provide the PIV in the diode	5		
3.	(a) What is a transistor? List its types. Also, write a note on the principle operation of a transistor with a neat sketch	5	2	2
	(b) Sketch neatly the BJT common emitter input and output characteristics curve. Also, write its h-parameter	5		

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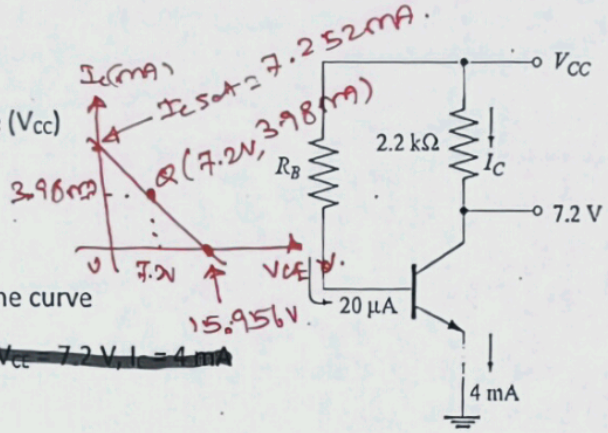
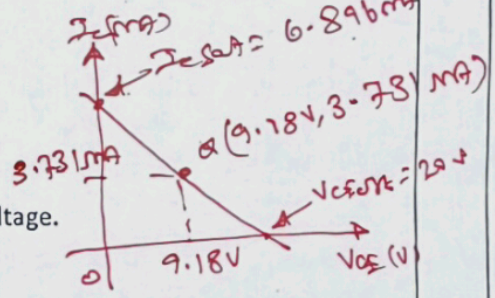
4.	Determine the following parameters for the given fixed-bias configuration shown in Fig. 2 a) Collector current (I_C) b) Collector bias voltage (V_{CC}) c) Current gain (β) d) Base resistor (R_B) e) Sketch the DC load-line curve ~~Assume: R_C = 2.2 kΩ, V_{CE} = 7.2 V, I_C = 4 mA and I_B = 40 μA~~  Fig. 2	10	2	3
5.	Determine the following parameters for the self-bias configuration: a) Base current and collector current b) Collector-emitter voltage c) Base voltage and Collector voltage, d) Collector saturation current and Cut-off voltage. e) Sketch the DC load-line curve Assume: V_{CC} = 20 V, V_{BE} = 0.7 V, R_B = 470 kΩ, R_C = 2 kΩ, R_E = 900 Ω and the current gain β = 110 	10	2	3

4. Fixed Bias configuration:

$I_E = I_B + I_C$

$\therefore I_C = I_E - I_B = 3.98$ mA.

$V_{CC} = (2.2\times10^{+3})(3.98\times10^{-3}) + 7.2$

$V_{CC} = 15.956$ V

$\beta = I_C/I_B = 199$

$R_B = \frac{V_{CC} - V_{BE}}{I_B} = 762.8$ kΩ

$I_{CSAT} = \frac{V_{CC}}{R_C} = 7.252$ mA

$V_{CE(OFF)} = V_{CC} = 15.956$ V.

$Q = (7.2\text{V}, 3.98\text{ mA})$

5. $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta)R_E} = 33.919\ \mu A.$

$I_C = 3.731$ mA.

$V_{CE} = V_{CC} - I_C(R_C + R_E) = 9.18$ V.

$V_B = V_{BE} + V_E = 4.057$ V.

$V_C = V_{CE} + V_E = 12.537$ V.

$I_{CSAT} = \frac{V_{CC}}{R_C + R_E} = 6.896$ mA.

$V_{CE(OFF)} = V_{CC} = 20$ V.

$Q = (9.18\text{V}, 3.731\text{ mA})$.