REG.NO.:

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - 1
WINTER SEMESTER 2025-2026

SLOT: D1+TD1

Programme Name & Branch : **B.Tech. & VLSI**
Course Code and Course Name : **BEVD207L - Computer Architecture**
Faculty Name(s) : **Arunachalam V, Dhanabal R**
Class Number(s) : **VL2025260500891, 0889**
Date of Examination : **30-January-2026**
Exam Duration : **90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes
  1. Understand the basic structure of computers, operations, and instructions.
  2. Understand the arithmetic and logic unit and implementation of fixed-point and floating-point arithmetic units.
  4. Understand the processor design control unit.

Q. No	Question	M	CO	BL
1.	List different streams of parallel computers according to Flynn's taxonomy. Explain each stream with the necessary block diagrams, which signify the operational units of it. *List: (a) SISD, (b) SIMD, (c) MISD, (d) MIMD* *Block diagrams with memory, CUs, PUs* *SISD, SIMD – 2 marks each* *MISD and MIMD – 3 marks each.*	10	1	1
2.	Consider two different machines, each with a distinct instruction set, that operate at a clock rate of 200 MHz. The following measurements are recorded on the two machines running a given set of benchmark programs:	10	1	3

Instruction Type	Instruction Count (millions)		Cycles per Instruction	
	Machine A	Machine B	Machine A	Machine B
Arithmetic & logic	8	10	1	1
Load and store	4	8	3	2
Branch	2	2	4	4
Others	4	4	3	3

Calculate the total execution time and compare these two architectures in terms of performance and speedup.

Total Execution time of machine A, $T_A = \frac{(8\times1)+(4\times3)+(2\times4)+(4\times3)}{200\times10^6} = 0.2\mu s$
Performance of machine A, $MIPS_A = \frac{18}{0.2\mu s} = 90\ MIPS$ (4 marks)

Total Execution time of machine B, $T_B = \frac{(10\times1)+(8\times2)+(2\times4)+(4\times3)}{200\times10^6} = 0.23\mu s$
Performance of machine A, $MIPS_A = \frac{24}{0.23\mu s} = 104\ MIPS$ (4 marks)

Speedup, $\frac{T_B}{T_A} = \frac{MIPS_B}{MIPS_A} = 1.15$; Machine A is 1.15 faster than B (2marks)

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3. Explain the Long/Restoring division algorithm with a necessary flow chart. 10 2 2
Verify the algorithm using the dividend, $Q = (-7)_{10}$ and divisor, $M = (3)_{10}$.
Q = 0111; M = 0011; -M = 1101

A	Q	C	
0000	0111	4	
0000 1101 0000	1110 1110	 3	Shift left A←A-M A<0, True, A←A + M
0001 1110 0001	1100 1100	 2	Shift left A←A-M A<0, True, A←A + M
0011 0000 0000	1000 1001	 1	Shift left A←A-M A<0, False, Q_0 = 1
0001 1110 0001	0010 0010	 2	Shift left A←A-M A<0, True, A←A + M

Q = 0010 ; Reminder = 0001

4. Represent the given numbers $A = (-0.45)_{10}$, and $B = (1.24)_{10}$ in Half precision floating-point format (*fp16*) as A_{fp16} and B_{fp16}. Also, determine $C_{fp16} = A_{fp16} + B_{fp16}$ using the floating-point addition algorithm. 10 2 3

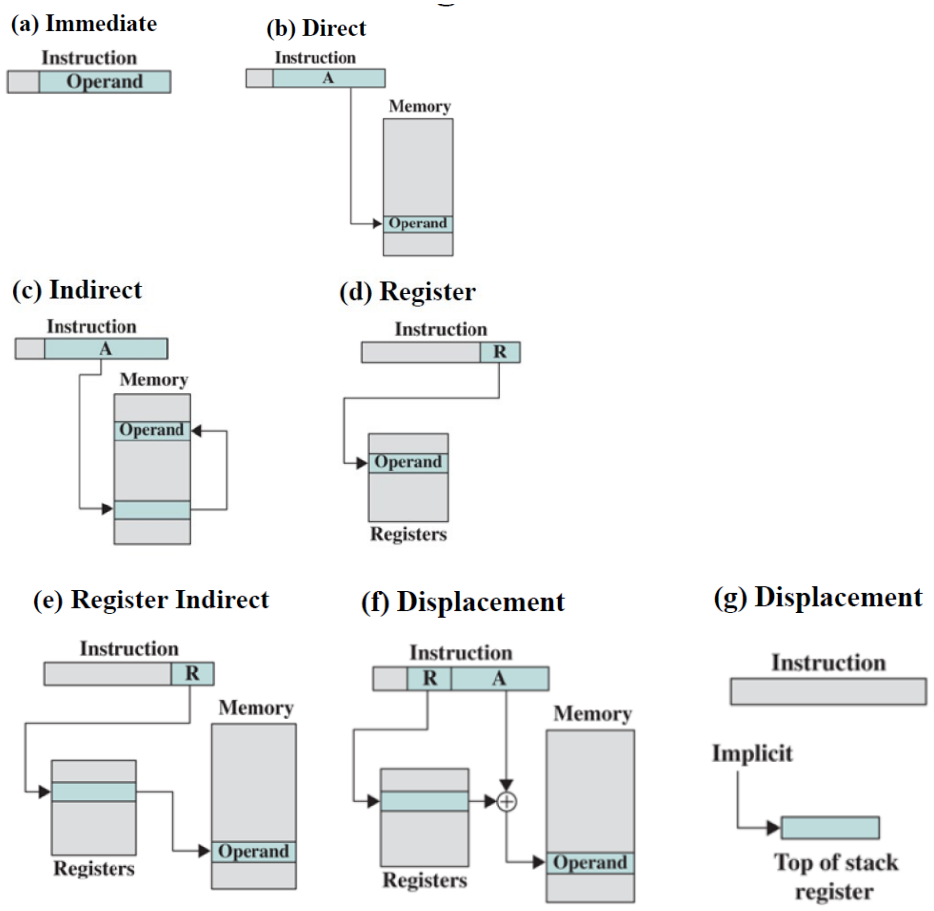
A = 0.45; 1.----×2^{-2} ; E_A = -2+15=13; 01101		
−1	0.8 × 2 = 1.6	1
−2	0.6 × 2 = 1.2	1
−3	0.2 × 2 = 0.4	0
−4	0.4 × 2 = 0. 8	0
−5	0.8 × 2 = 1.6	1
−6	0.6 × 2 = 1.2	1
−7	0.2 × 2 = 0.4	0
−8	0.4 × 2 = 0. 8	0
−9	0.8 × 2 = 1.6	1
−10	0.6 × 2 = 1.2	1
A_{f16} = <1><01101><1100 1100 11>		

B = 1.24; 1.----×2^{0} ; E_B = 0+15=15; 01111		
−1	0.24 × 2 = 0.48	0
−2	0.48 × 2 = 0.96	0
−3	0.96 × 2 = 1.92	1
−4	0.92 × 2 = 1.84	1
−5	0.84 × 2 = 1.68	1
−6	0.68 × 2 = 1.36	1
−7	0.36 × 2 = 0.72	0
−8	0.72 × 2 = 1.44	1
−9	0.44 × 2 = 0.88	0
−10	0.88 × 2 = 1.76	1
A_{f16} = <0><01111><0011 1100 01>		

$$B \rightarrow 1.0011\ 1101\ 01 \times 2^{0}$$
$$B \rightarrow 100.1111\ 0101\ 00 \times 2^{-2}$$
$$A \rightarrow 1.1100\ 1100\ 11 \times 2^{-2}$$
$$C = B - A \rightarrow (100.1111\ 0101\ 00 - 1.1100\ 1100\ 11) \times 2^{-2}$$
$$C = B - A \rightarrow (011.0010\ 1000\ 01) \times 2^{-2} = (1.1001\ 0100\ 00) \times 2^{-1}$$

C_{f16} = <0><01110><1001 0100 00>

5.	List and explain the basic addressing modes used in a general computer architecture, providing necessary illustrations such as instruction formats and memory maps.	10	4	1



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