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Reg. No:

Final Assessment Test – April 2025

VIT
Vellore Institute of Technology

Course: BITE301L - Computer Architecture and Organization
Class NBR(s): 2702 / 2716 / 2721
Slot: A1+TA1
Time: Three Hours
Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

Answer ALL Questions
(10 X 10 = 100 Marks)

1.(a) i) List the steps needed to execute the machine instruction: [6]

MUL LOCA,R2 in terms of transfers between the components of processor. Assume that the address of the memory location containing this instruction is initially in register PC.

ii) Analyse the status of the condition code flags when the following instruction is executed. Add R4, R5 where **R4=$(CE)_{16}$, R5=$(AB)_{16}$** [4]

OR

1.(b) i) Program execution time T is to be examined for a certain high-level language program. The program can be run on a RISC or a CISC computer. Both computers use pipelined instruction execution, but pipelining in the RISC machine is more effective than in the CISC machine. Specifically, the effective value of S in the T expression for the RISC machine is 3.2, but it is only 4.5 for the CISC machine. Both machines have the same clock rate R.

1) What is the largest allowable value for N, the number of instructions executed on the CISC machine, expressed as a percentage of the N value for the RISC machine, if time for execution on the CISC machine is to be longer than on the RISC machine? [4]

2) Repeat Part (1) if the clock rate R for the RISC machine is 13 percent higher than that for the CISC machine. [2]

ii) Explain with neat diagram about bus structures and write the drawbacks of single bus structure. [4]

2. a) Represent the integer 16537 in Big Endian and Little Endian machine (32-bit). [6]

b) Write an Assembly Language Program to find the average of N numbers using Assembler Directives. [4]

3. Assume that an instruction is stored at the location 2000 with its address field at location 2001. The address field has the value 1000. The processor register R1 = 1200, XR = 1255, PC= 900, and BR =800.

Address	Value
1000	2100
1100	2200
1199	2255
1903	2280
1200	2300
1201	2355
1800	2485
2100	2500
2200	2600
2255	2655

Write the instruction of the given addressing mode to evaluate the effective address and find out the content of AC for the given data if the addressing mode of the instruction is,

a) Immediate addressing mode
b) Direct addressing mode
c) Indirect addressing mode
d) Register addressing mode
e) Register indirect addressing mode
f) Pre and post increment addressing mode
g) Pre and post decrement addressing mode
h) Relative addressing mode
i) Indexed addressing mode
j) Base register addressing mode

4. Assume that you are designing a special control unit in order to transfer a block of data directly between an I/O device and the main memory, without continuous intervention by the processor. Explain the role of DMA controller in this system.

5. Design 2048 × 16 – bit RAM using 2048 × 8 – bit RAM chips and 1024 × 8 – bit ROM using 512 × 8 – bit ROM chips.

i) Draw the memory map table [5]

ii) Draw memory design diagram [5]

6. Consider a cache memory of size 2048MB with block size 256 bytes. The size of main memory is 256 GB. Find the physical address splits for,

a) Direct mapping [3]

b) Associative mapping [3]

c) 4-Set associative mapping [4]

7.(a) Demonstrate the step by step multiplication process using binary multiplication algorithm, when the following numbers are multiplied. B = 46 (Multiplicand) Q = 15 (Multiplier). Use 6-bit register to store the values. Show the contents of the register E,A,Q and SC during the multiplication process. Draw the necessary flow diagram.

OR

7.(b) Divide 48 by 14 using division and storing algorithm and find out the value of the quotient and remainder with proper sign. Show the contents of the registers E, A, Q & SC during the process of a division. Draw the necessary flow diagram.

8. a) Formulate the value of 16.565 in 32-bit and 64-bit floating point format IEEE 754. [5]

b) Perform the arithmetic operations below with binary numbers and with negative numbers in signed Magnitude representation. In each case determine if there is an overflow. Use 6 bits register to accommodate each number. [5]

(i) (+15) + (+40) ii) (-15) + (+40)

9. a) An instruction pipeline consists of 4 stage Fetch (F), Decode fields (D), Execute (E) and result Write (W). Assume that each instruction requires different stage delay (in terms of number of clock cycles) as mentioned in the table below, [5]

Instruction	F	D	E	W
1	2	1	1	1
2	1	2	2	1
3	3	2	1	2
4	1	2	3	2
5	2	3	1	2
6	3	2	2	1

Find the number of clock cycles needed to complete these six instructions in the given pipelining system.

b) Consider the following sequence of instructions [5]

Add #30,R0,R1

Mul #4,R2,R3

And #$4A,R2,R4

Add R0,R2,R5

In all instructions, the destination operand is given last. Initially, registers R0 and R2 contain 1500 and 150, respectively. These instructions are executed in a computer that has a four-stage pipeline. Assume that the first instruction is fetched in clock cycle 1, and that instruction fetch requires only one clock cycle.

Describe the operation being performed by each pipeline stage during each of clock cycles 1 through 4, with the help of a diagram.

10. a) Explicate with neat sketch about the structure of general-purpose multiprocessor. [5]

b) Elucidate with neat sketch about any 4 Interconnection networks. [5]

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