SLOT: B1+TB1

VIT

Vellore Institute of Technology

School of Computer Science Engineering and Information Systems (SCORE)

CONTINUOUS ASSESSMENT TEST – I
WINTER SEMESTER 2024-2025

Programme Name & Branch	:	**B.Tech (IT)**
Course Code and Course Name	:	**BITE202L Digital Logic and Microprocessors**
Faculty Name(s)	:	**Dr.NITHYA.S Dr.SANTHI K Dr.PRADEEPA M Dr.KRISHNAMOORTHY N**
Class Number(s)	:	**VL2024250502963/2973/2971/2958**
Date of Examination	:	**28.01.2025**
Exam Duration	:	**:90 minutes** **Maximum Marks:50**

General instruction(s):

Answer All Questions

- Answer All Questions
  M- Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply,4 – Analyse,5 – Evaluate,6 – Create)
- Course Outcomes

  1. Understanding the structure of various number systems and Illustrate simplification of Boolean functions to achieve optimized design of digital logic circuits.
  2. Demonstrate the design, and analysis of various combinational logic circuits and sequential logic circuits using flip flops and logic gates.

Q.No	Question	M	CO	BL
1.	i. Convert the Hexadecimal number 2D5.A3 into binary. ii. Convert the Hexadecimal 68BE to octal. iii. Convert the binary number 01011, into a Gray Coded number. iv. Obtain 1's and 2's complement a) 11011010 b) 10000101	10	CO1	2
2.	Assume a manufacturing plant needs to have a horn sound to signal quitting time. The horn should be activated when either of the following conditions is met: • Its after 5 o 'clock and all machines are shut down. • Its Friday, the production run for the day is complete, and all machines are shut down. Design a logic circuit that will control the horn.(Hint: use four logic input variables to represent the various conditions, for example, input A will be High only when the time of day is 5 o'clock or later) Design a combinational circuit for the above mentioned scenario.	10	CO1	3
3.	a. Implement the following Boolean expression using NOR only. F=(A+B+C') (A+B') (A+B'+C'')	5	CO2	4
	b. Design a logic circuit which acts as full adder and full subtractor based on a control input. If the control input is '0'', the circuit will act as adder else subtractor. Implement using basic gates.	5		

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4.	Simplify the following Boolean function F, together with the don't-care conditions. $F(A,B,C,D) = \sum(2, 4, 10, 12, 14) + d(A,B,C,D) = \sum(0, 1, 5, 8)$. Assume that both the normal and complement inputs are available.	10	CO1	5
5.	Using 2x4 decoders and one 4x1 mux, design a circuit with the following properties. It has two 2-bit binary inputs [x1 x0] [y1 y0] and It has following four output modes to select the function of the circuit i. EQ outputs a 1 if two inputs are equal ii. GTE outputs a 1 if X is larger than Y iii. LTE outputs a 1 if the X is smaller or equal to Y iv. NULL outputs a 0 You must use minimum number of 2x4 decoders with enables (i.e. if the enable is 0 all the outputs of the decoder are 0, otherwise, the output is 1 for the respective minterm), only one 4x1 mux and a minimum number of additional gates. Show the circuit diagram with all the pins to the decoders and mux labelled properly. State any assumptions you are making in your design.	10	CO2	3

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