VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science and Engineering

Winter Semester 2023-24

Continuous Assessment Test – II

SLOT: D2+TD2

Programme Name & Branch: BCB, BCE, BCI, BCT, BDS, BKT

Course Name & Code: Computer Architecture and Organization- BCSE205L

Class Number (s): Common to all

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Answer all five questions

Q. No.	Question	Max Marks
1.	A program runs in 10 seconds on computer X with 2 GHz clock. Assume that the Computer Y runs the same program in 6 seconds, then compute the following: i)What is the number of CPU cycles on computer X ? ii) If computer Y requires 10% more cycles to execute program when compared to computer X, then what is the clock rate for computer Y? iii) Assume the computer Z is running with clock rate of Y and the number of clock cycles as X, then find the CPU time of Computer Z. iv) Identify the fastest and slowest machine among X, Y and Z. v) Assume that the computer A executes 3 million instructions in the CPU time of the fastest Computer among X, Y and Z, determine MIPS. **Solution:** i) CPU cycles on computer X = 10 sec $\times 2 \times 10^9$ cycles/s = 20×10^9 cycles ii) CPU cycles on computer Y = $1.1 \times 20 \times 10^9 = 22 \times 10^9$ cycles Clock rate for computer Y = 22×10^9 cycles / 6 sec = 3.67 GHz iii) Clock rate of computer Z = 3.67 GHz = 3.67×10^9 No. of clock cycles of Z= 20×10^9 cycles CPU time of computer Z = 20×10^9 cycles / 3.67×10^9 = 5.44s v) CPU time of X = 10 s CPU time of Y = 6s CPU time of Z = 5.4495 s Therefore, faster machine is, Computer Z slower machine is, Computer X iv) Instruction count of computer Z = 3 million MIPS rating = 3 / 5.44 = 0.551470 s	10

2. A computer employs RAM chips of 1024 x 8 and ROM chips of 1024 x 8. The computer system needs 2k *8 bytes of RAM, 2k *8 bytes of ROM, and four interface units with four registers in each. A memory-mapped I/O configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers. **10**

a. How many RAM and ROM chips are needed?
b. Draw a memory-address map for the system.
c. Give the address range in hexadecimal for RAM, ROM, and interface.
d. Develop a chip layout for the above said specifications.

Solution:

No. of Chips and Address Calculation

S.NO	Memory	N x W	N^1 x W^1	P	Q	p*q	x	y	z	Total
1	RAM	1024 x 8	2048 x 8	2	1	2	10	1	2	13
2	ROM	1024 x 8	2048 × 8	2	1	2	10	1	2	13
3	Interface	4		4	1	4	2	2	2	6

a) No. of RAM chips are needed (**p*q**): 2
and No. of ROM chips are needed : 2

b) Memory Address Map:

Component	c) **Hexadecimal Address**			Address Bus											
	From	To	13 - 15	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM 1	0000	03FF		0	0	0	x	x	x	x	x	x	x	x	x	x
RAM 2	0400	07FF		0	0	1	x	x	x	x	x	x	x	x	x	x
ROM 1	0800	0BFF		0	1	0	x	x	x	x	x	x	x	x	x	x
ROM 2	0C00	0FFF		0	1	1	x	x	x	x	x	x	x	x	x	x
Interface 1	1000	1003		1	0	0	0								x	x

Interface 2	1200	1203		1	0	0	1								x	x
Interface 3	1400	1403		1	0	1	0								x	x
Interface 4	1600	1603		1	0	1	1								x	x

d) Chip layout

Design Diagram (2m)

3. Consider a 2-way set associative cache memory with total 8 cache lines and a main memory with 128 blocks. Assume that the cache is initially empty. Which memory references will be present in the cache if optimal cache block replacement policy is used with the following sequence of memory references? Compute the Hit ratio (H) and Miss ratio (M). — 10

Memory references are: 5, 2, 3, 7, 3, 15, 14, 2, 1, 21, 13, 72, 12, 5, 19, 3, 2, 1, 22, 9, 26, 10, 5, 1, 7, 26, 14, 9, 19, and 26.

Solution:

Set 0	72	12
Set 1	~~5~~ 1	~~1~~ ~~21~~ ~~13~~ ~~1~~ 9
Set 2	~~2~~ ~~22~~ 26	~~14~~ ~~10~~ 14
Set 3	~~3~~ 7	~~7~~ ~~15~~ 19

Therefore, memory references will be present in the cache are:

72, 12, 1, 9, 26, 14, 7, 19

Hit Ratio = 10 / 30 = 0.33 %

Miss Ratio = 0.67 %

4. a) A hard disk with a transfer rate of 10 Mbytes/seconds is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation? — 10 (5+5)

Solution:

DMA transfer rate = 10 MBps = $10 \times 10^6 = 10^7$ bytes per second
Processor frequency = f = 600 MHz = $600 \times 10^6 = 6 \times 10^8$ Hz
No. of cycles used by CPU = 300 + 900 = 1200
Block size = 20KB = $20 \times 10^3 = 2 \times 10^4$ bytes

Time consumed by CPU = No. of cycles used by CPU / Processor frequency
$= 1200 / (6 \times 10^8) = 2 \times 10^{-6}$ sec
Time consumed by DMA = Block size / DMA transfer rate
$= 2 \times 10^4 / 10^7 = 2 \times 10^{-3}$ sec

$$\% \text{ of time consumed by the CPU} = \frac{\text{Time consumed by CPU}}{(\text{Time consumed by CPU} + \text{Time consumed by DMA})} \times 100$$

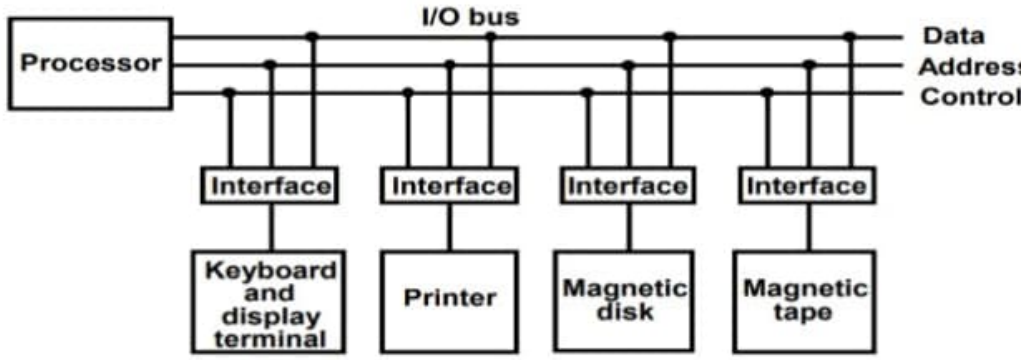
$$= \frac{2 \times 10^{-6}}{(2 \times 10^{-6}) + (2 \times 10^{-3})} X100 = \frac{2 \times 10^{-6}}{(2 \times 10^{-6}) + (2000 \times 10^{-6})} X100$$

$$= 0.0999\ \% = 0.1\%$$

b) Discuss the functionality of interfaces in I/O subsystem with neat diagram.
Key points:

- Each peripheral has an interface module to get connected with the computer system.
- Each Interface decodes the address and control received from the I/O bus, interprets them for peripherals and provides signals for the peripheral controller.
- It is also synchronizes the data flow and supervises the transfer between peripheral and processor.
- Each peripheral has its own controller.

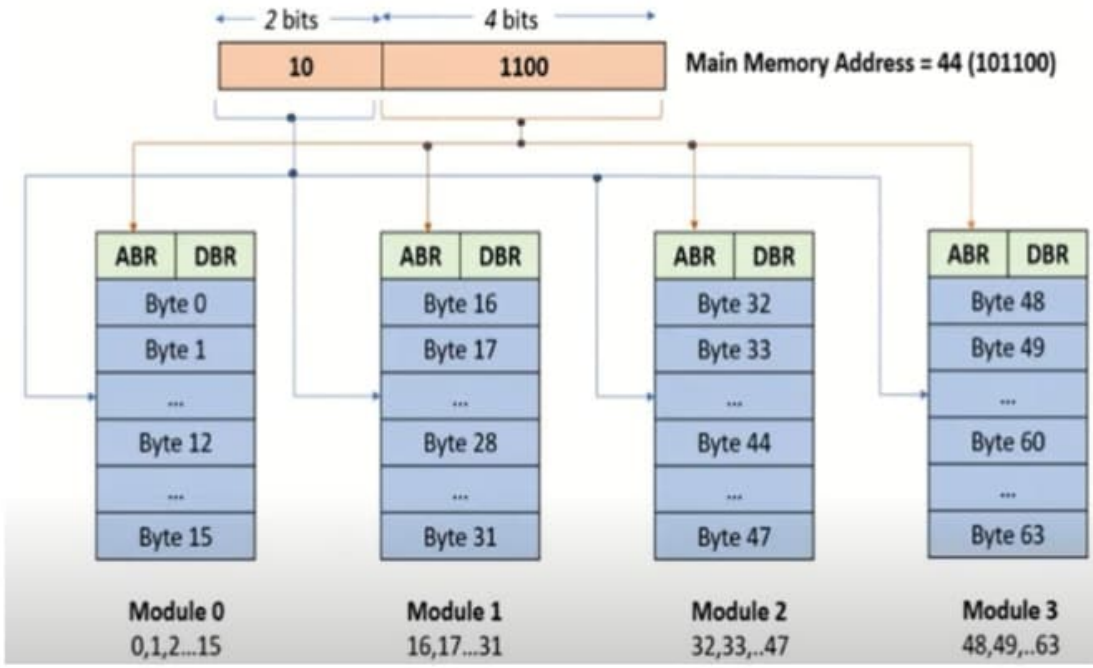
Diagram



Note: Expected to explain

5.	a) Consider a byte addressable memory of 64 bytes with 4 way high-order interleaved. Determine the following: i) If the CPU generates 101100 main memory address, then identify the bits required to select the module and the bits required to select the specific location in the selected module. Also mention the selected module and specific location in the selected module for the above mentioned address. ii) Sketch the structure of the above interleaved main memory. **Solution:** **Given, 4 way interleaving = 4 modules = 2^2** **Modules are labeled as m0, m1, m2, and m3** i) Bits required to select the module = 2 For High order interleaving, high order 2 bits are required to identify each module. Given main memory address = 101100 **Therefore, Module bits to be used is = 10 (i.e.m2)** Bits required to select the specific location in the selected module = 1100 (LSB bits) Selected module is m2 (module 2) Specific location in the selected module : Byte 44 (13^{th} location in module 2)	10 (5+5)

ii) Structure

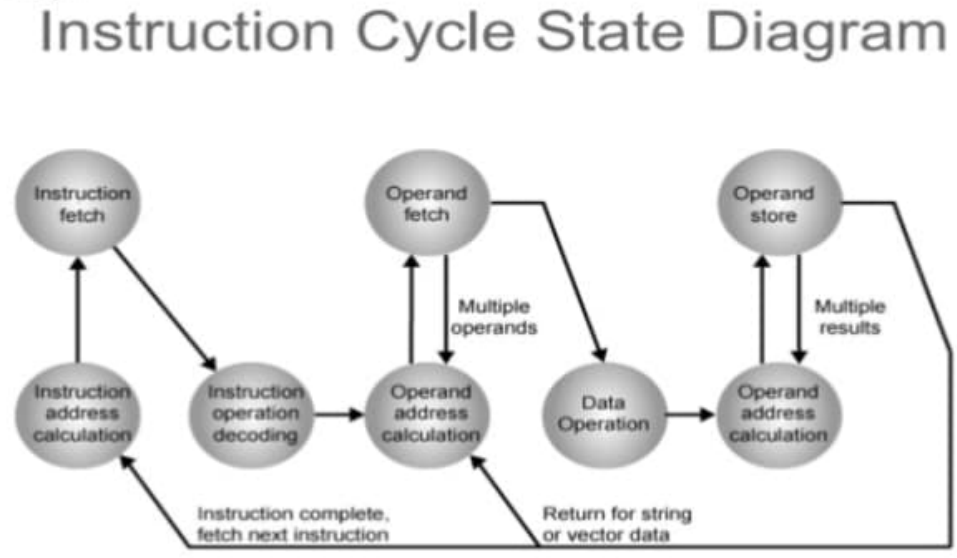


b) Explain different phases of instruction cycle with neat sketch. Describe the various CPU registers involved for the completion of each instruction execution.

Different phases are:

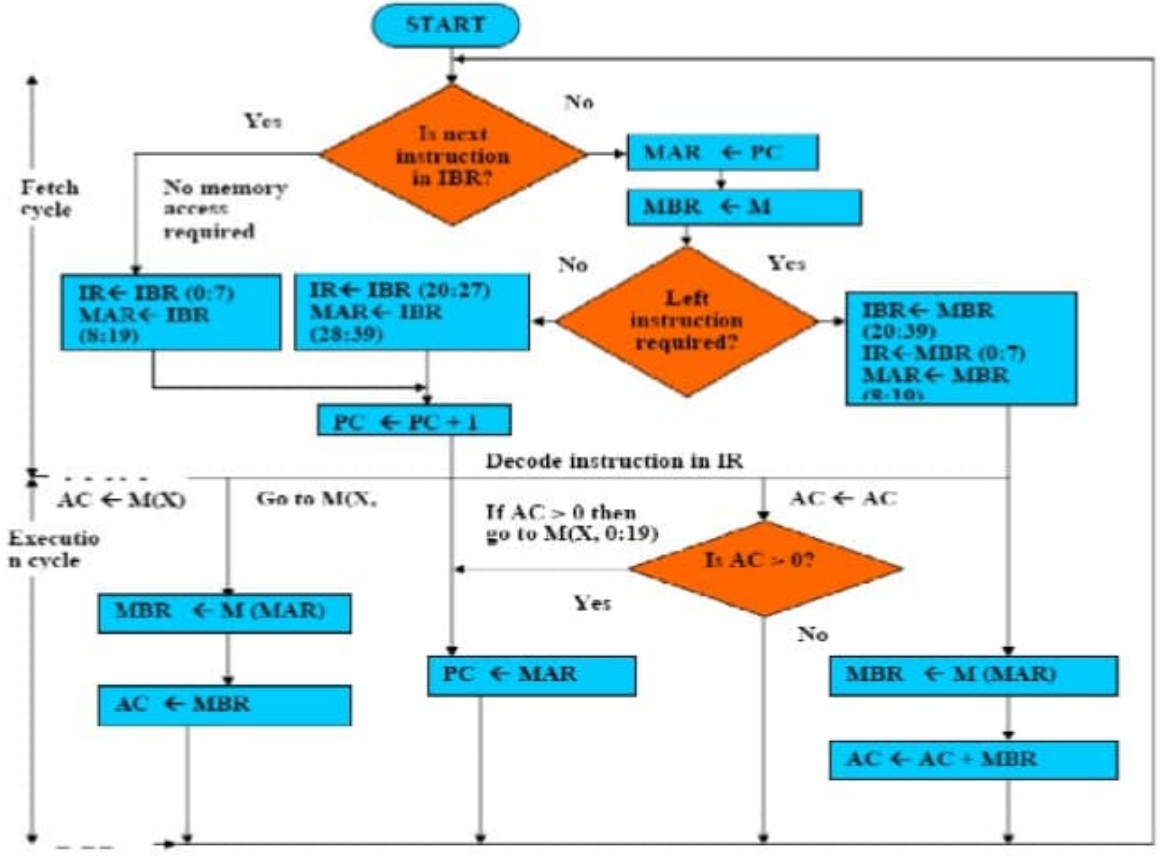
- Fetch stage
- Decode stage
- Execute stage

Diagram



Note: Expected to explain each phase

(Or)



CPU Registers involved:

- Program Counter
- Memory Address Register
- Memory Data Register
- Instruction Register
- Accumulator