Reg. No: 23BEC0173

D/L/TX

VIT® Vellore Institute of Technology

Final Assessment Test – November 2024

Course: BECE102L - Digital Systems Design

Class NBR(s): 3667 / 3674 / 3679 / 4051 / 4054 Slot: D2+TD2

Time: Three Hours Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXA MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

Answer ALL Questions

(10 X 10 = 100 Marks)

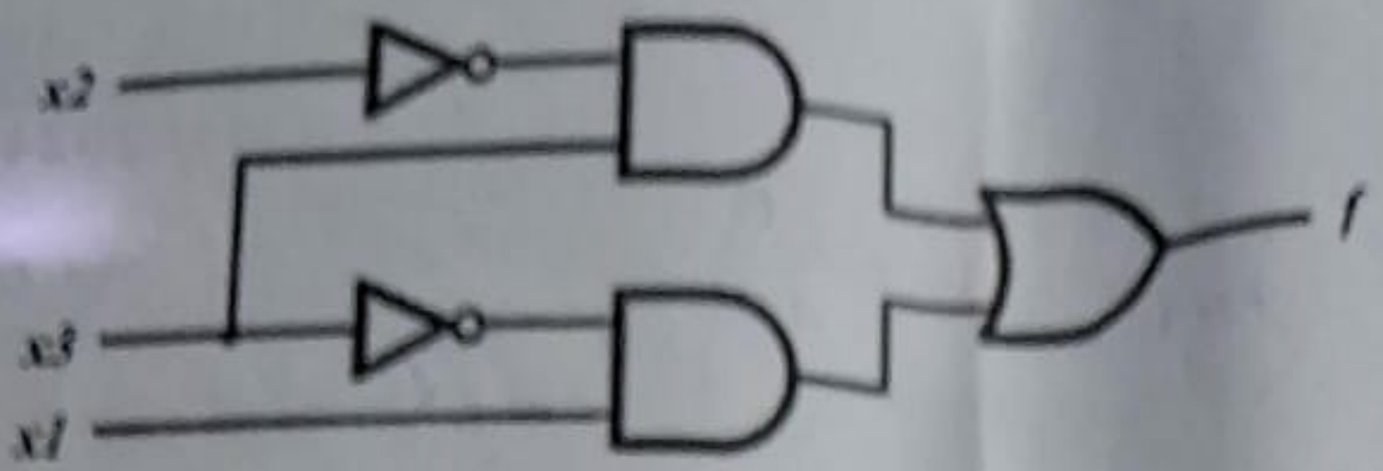
1. Simplify the Boolean expression $F= (w + y) (wz + w\overline{z}) + wy + y$ and realize the reduced expression in CMOS logic.

2. Draw the logical diagram of simplified SOP and POS for the Boolean function $F(A,B,C,D) = \Sigma(1,3,5,7,9,15) + d(4,6,12,13)$, where 'd' represents the don't care conditions.

3. Draw the logic diagram of the digital circuit specified by the following gate level verilog description and rewrite the code in dataflow modelling.

```
module Q3_Circuit (A, B, C, D, F);
    input A, B, C, D;
    output F;
    wire w, x, y, z, a, d;
    or (x, B, C, d);
    and (y, a ,C);
    and (w, z ,B);
    and (z, y, A);
    or (F, x, w);
    not (a, A);
    not (d, D);
endmodule
```

4. Construct the verilog code for the circuit shown below in gate level modeling. Sketch the output waveform for the circuit if the input (x3, x2, and x1) transition occurs from 101 to 011 in 7ns. Assume that each NOT, AND and OR gate has a propagation delay of 3ns, 5ns and 4ns respectively.



5. Implement the Boolean function $F(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$ using

mod - 3

(a) 8x1 multiplexer with A, B, C as select signals and

(b) 3 to 8 decoders with additional basic gates.

6. Assume that a 6-bit registers A and B of the sequential Booth's multiplier are initialized with the values -15 and 10.

i. Show the steps of multiplication operation according to Booth's algorithm.

ii. After multiplication, how many subtraction and addition operations will be performed?

7. A PQ flip-flop has four operations, no change, reset, set and complement, when inputs P and Q are 00, 10, 01 and 11, respectively.

(a) Determine the characteristic table of the flip-flop.

(b) Find the characteristic equation of the flip-flop.

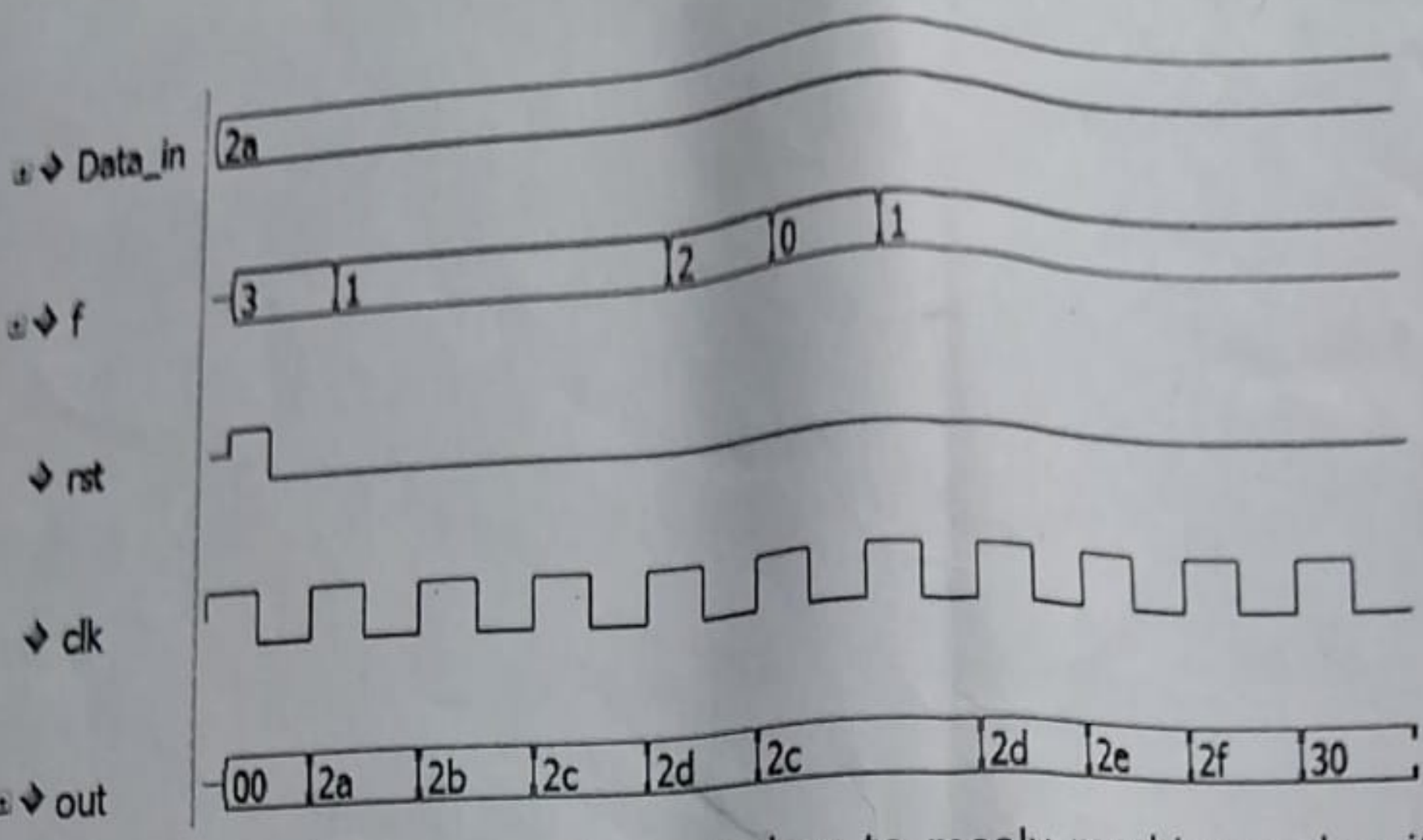
(c) Determine the excitation table.

(d) Convert the flip-flop to a D flip-flop.

8.(a) Design a sequential circuit which transit through the following states 000, 100, 110, 111, 011, 001, and (repeat) 000 using T Flip-Flops

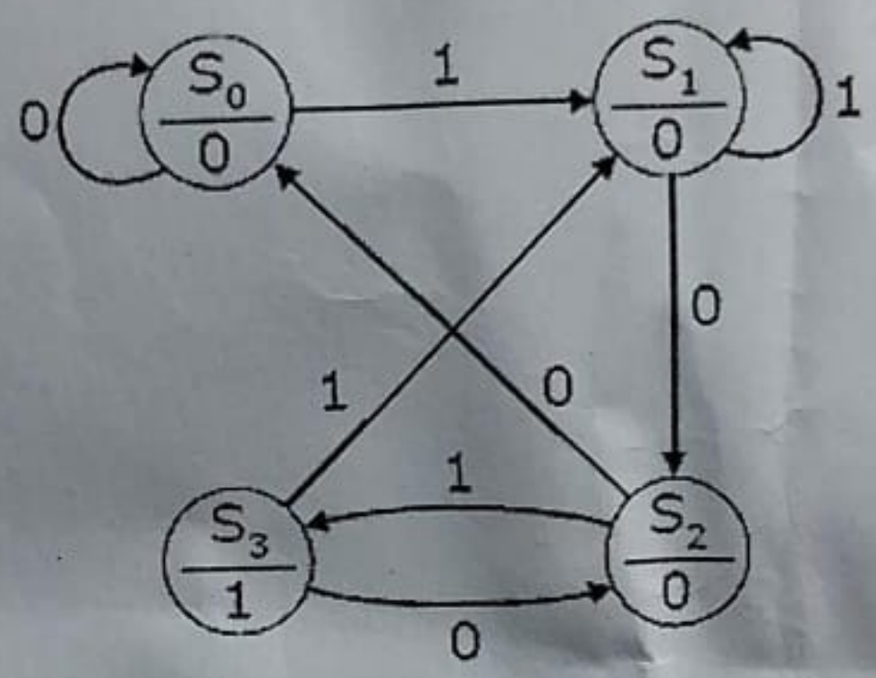
OR

8.(b) Develop sequential circuit in behavioral modelling to generate the following waveform as shown below with Data_in as a 6-bit input, f is the control signal and out is the output of the circuit.



9.(a) Convert the state diagram shown below to mealy machine and write the behavioural Verilog code for the design using D-Flip flop.

→ FSM



OR

9.(b) You want to build a Mealy based finite state machine using behavioural Verilog code that will recognize the sequence X = 1101 and output Z = 1 when this sequence occurs. Allow overlap of sequences.

10 Implement the following Boolean functions using the PLA and PAL device.

a) $F(A, B, C) = \Sigma m(0,3,5,4,7)$

b) $G(A, B, C, D) = \Pi M\ (0, 2, 3, 4, 5, 8, 10, 11, 15)$

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