



SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

Programme Name & Branch : B.Tech & common to all
Course Code and Course Name : BCSE205L & Computer Architecture and Organization
Faculty Name(s) : Common to all
Class Number(s) : Common to all
Date of Examination : 27.01.2026
Exam Duration : 90 minutes

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO - Course Outcome; BL - Blooms Taxonomy Level (1 - Remember, 2 - Understand, 3 - Apply, 4 - Analyse, 5 - Evaluate, 6 - Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)

CO1- Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.

Q. No	Question	Module	Marks	CO	BL
1.	a) Consider the following expression using the IAS computer instruction set and interpret the flow of the IAS computer architecture (Register flow of operations) with neat diagram. $K = (M + N) - O$ Assume the memory locations 900, 901, and 902 for M, N, and O respectively.	1	7	1	BL 1
	b) Compare and contrast Von Neumann and Harvard computer architectures.	1	3	1	BL 1
2.	Perform 21/11 using Restoring division algorithm and explain the steps clearly and draw the flowchart.	2	10	1	BL 3
3.	a) Using Booth's algorithm, multiply $(+12) \times (-5)$ with a neat flowchart.	2	7	1	BL 3
	b) Describe the structure and components of IEEE 754 single-precision and double-precision floating-point formats with neat diagrams.	2	3		
4.	a) Consider the following instructions, classify each into the appropriate instruction set category and justify your answer: i) MOV R1, R2	3	5	1	BL 3



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	ii) ADD R3, R4 iii) JMP 200 iv) IN PORT1 v) NOP vi) AND R5, R6 vii) BCD to Binary Conversion viii) LOAD R1, M[150]				
	b) With neat diagram, explain how CPU, Memory, and I/O devices are interconnected in a computer system.	1	5		
5.	Convert the following expression into assembly instructions for 0,1,2,3 address formats and calculate the total memory traffic: $P = (Q \times R) - S$ Use the same assumptions: - Address: 2 bytes - Data: 2 bytes - Opcode: 8 bits - Word length: 1 byte	3	10	1	BL 3
