Assignment - 2

1. In the circuit given in Fig.(1) the silicon transistor has β=71 and $V_{BE(on)}$=0.7V. If V_c =9V, the ratio of R_B and R_C is:

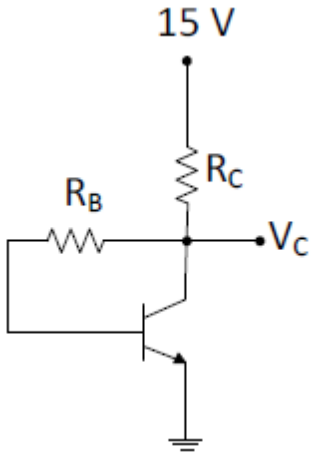

Fig.(1)

2. In the circuit given in Fig.(2), the transistor is in active mode and V_C=2V. To get V_C=4V we replace R_C by R_{CA}. The ratio R_{CA}/R_C is:

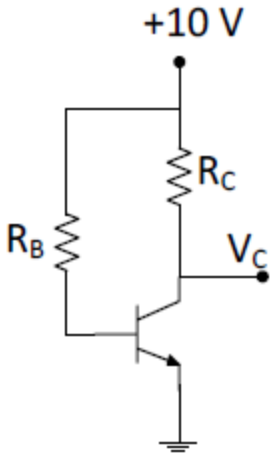

Fig.(2)

3. Consider the circuit shown in Fig.(3). Find the incremental resistance measured between the terminals A and B, taking the $\beta = \infty$.

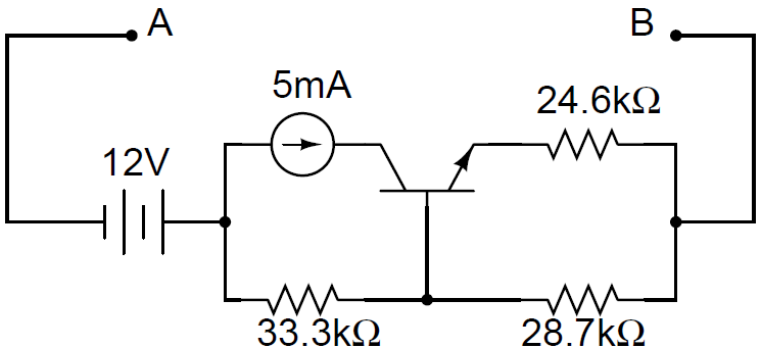

Fig.(3)

4. In the circuit shown in Fig.(4), 10V is considered logic '1' and 0V as logic '0'. What gate does it implement?

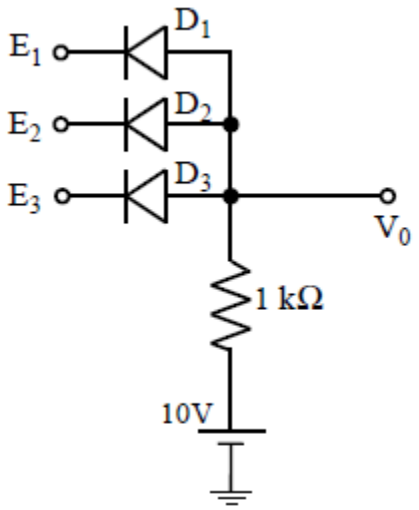

Fig.(4)

5. A piece of silicon is doped uniformly with phosphorous with doping concentration of $10^{16}cm^{-3}$. The expected value of mobility versus doping concentration for silicon assuming full ionization is given in the chart below (see Fig.(5)). The conductivity of the silicon sample at 300K is _____.

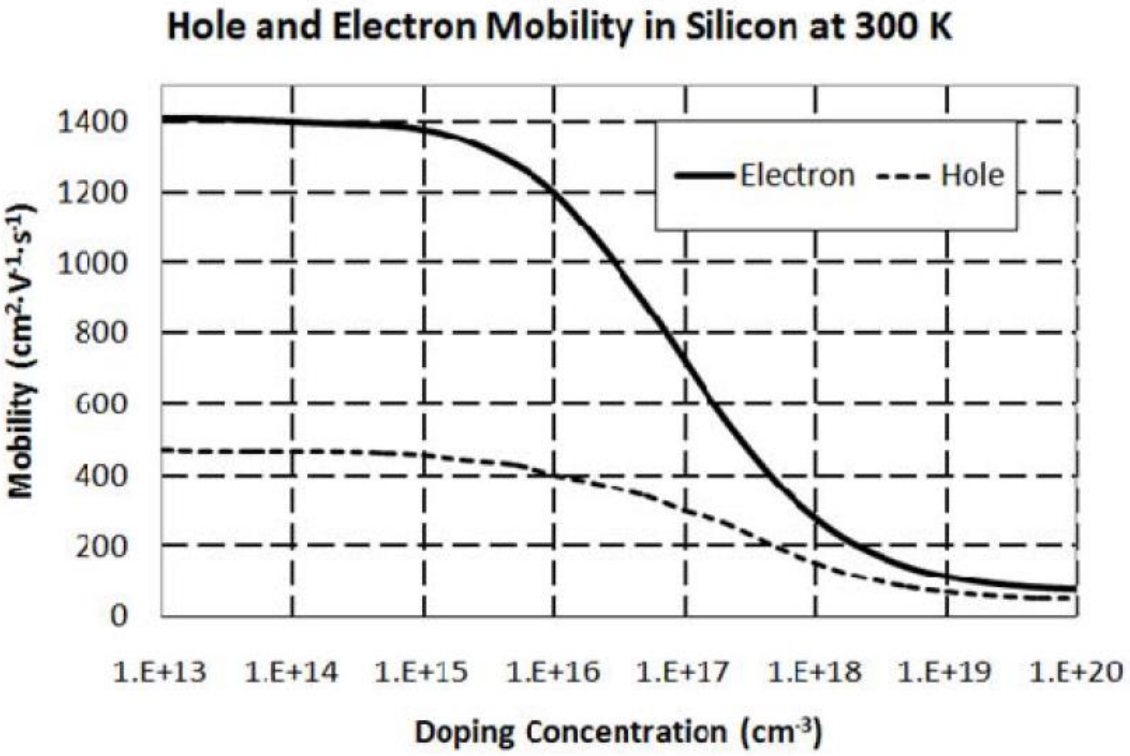

Fig.(5)

General Instructions: Solve the problems after reading the questions very carefully. Few problems consume much more thinking and time.

Format: Handwritten. Scan and upload PDF only. Before uploading, check if your file opens properly. If I find that your file is corrupt and does not open, you will be given zero.

Note: Digital copying (taking snapshots of somebody else's work) will lead to severe penalties. Write your own assignment, take photo and upload. It is okay to discuss with classmates, but the submission has to be original. Take it as a learning exercise. Do not miss deadlines; offline submission is not accepted.

Best wishes……..