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Vellore Institute of Technology

Final Assessment Test – April 2023

Course: **BECE102L - Digital Systems Design**

Class NBR(s): **6857** Slot: **X11+X12+X21**

Time: **Three Hours** Max. Marks: **100**

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS TREATED AS EXAM MALPRACTICE

Answer any TEN Questions

(10 X 10 = 100 Marks)

1. Simplify the Boolean function to minimum literals
   a) ABC + A'B + ABC'
   b) (A' + C') (A + B' +C')

2. Draw the logic diagram of the digital circuit specified by the following Verilog description

```
module circuit_unknown (F1,F2,F3,A0,B0, B1);
  output F1,F2,F3;
  input  A0, A1,B0,B1;
  nor    (F1,F2,F3);
  or     (F2,w1,w2,w3);
  and    (F3,w4,w5);
  and    (w1,w6,B1);
  or     (w2,w6,w7,B0);
  and    (w3,w7,B0,B1);
  not    (w6,A1);
  not    (w7,A0);
  xor    (w4,A1,B1);
  xnor   (w5, A0, B0);
endmodule
```

3. Simplify the following Boolean functions, using four-variable K- maps
   a) F(A,B,C,D) = Σm(1,4,5,6,12,14,15)
   b) F(A,B,C,D) = Σm(2,3,6,7,12,13,14)

4. Draw the logic diagram of a 2-to-4 line decoder using
   (a) NOR gates only and (b) NAND gates only and write its truth table.

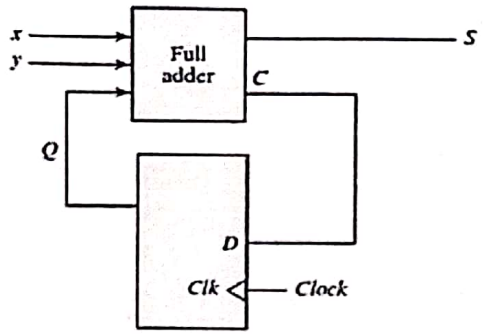
5. Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-to4-line decoder.

6. Design a 4-bit shift Register using T-FF. The contents of a four-bit register are initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift?

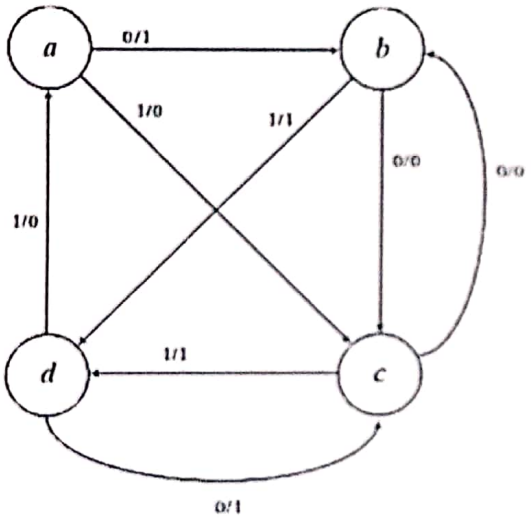
7. Design a for 4-bit binary ripple countdown counter and Draw the logic diagram of a four-bit binary ripple countdown counter using D-flip-flops that trigger on the positive-edge of the clock.

8. Design a circuit that detects 3 or more ones in a string of bits coming through an input line.
   (Using either Mealy or Moore FSM)

9. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in Figure. Derive the state table and state diagram of the sequential circuit.



10. Write a Verilog model of the Mealy FSM described by the following figure. Develop a test bench and demonstrate the machine state transitions and output correspond to its state diagram.



11. Obtain the expression for C1, C2, C3 and C4 for a four bit carry look ahead adder circuit. Write the verilog code for a 16 bit carry look ahead adder using 4 bit CLA module instantiation.

12. Derive the PLA programming table for the combinational circuit that squares a three-bit number. Minimize the number of product terms.

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