

**Final Assessment Test – November 2025**

Course: BECE102L - Digital Systems Design

Class NBR(s): 2573 / 2579 / 3578 / 3580 / 3583 / 3585 /

3587 / 3589 / 3591 / 3593 / 3598 / 3600 / 3603 / 3605 /

3608 / 3610 / 3613 / 3619 / 3622 / 3627 / 3630 / 3634 /

3643 / 3645 / 3647 / 3651 / 3657

Slot: F1+TF1

Time: Three Hours

Max. Marks: 100

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

COs	CO Statements
CO1	Optimize the logic functions using and Boolean principles and K-map.
CO2	Model the Combinational and Sequential logic circuits using Verilog HDL.
CO3	Design the various combinational logic circuits and data path circuits.
CO4	Analyze and apply the design aspects of sequential logic circuits.
CO5	Analyze and apply the design aspects of Finite state machines.
CO6	Examine the basic architectures of programmable logic devices.

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 = Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions

(10 X 10 = 100 Marks)

1. (i) Draw the CMOS logic circuit for the Boolean function  $F = \overline{(A + B)(C + D)}$ . CO1 BL3
- (ii) Implement the Boolean function  $F(x, y, z) = \sum m(2,3,5,7)$  using NAND gates only.
2. Find the simplified SOP and POS for the function  $F(w,x,y,z) = \sum m(0,2,3,6,7)$  with don't care  $d(w,x,y,z) = \sum d(8,10,11,15)$  and draw the logic diagram using logic gates. CO1 BL3
3. Develop a structural level Verilog code to implement 4:1 MUX using 2:1 MUX and also write the testbench. CO2 BL3
4. Implement the Boolean function  $F(a, b, c) = a(b + c') + a'bc$  using a 4:1 MUX and consider the select signals as a and c. CO3 BL3
5. Design a 3-bit combinational circuit that converts binary input to Excess-1 output. For example, if the input is '011' which generate the output as '100'. Draw the corresponding truth table and logic diagrams. CO3 BL3
- 6(a) Develop a structural verilog code for a 4-bit adder/subtractor circuit. CO2 BL3

OR

- 6(b) Design a three bit magnitude comparator and write a verilog code in Behavioural modeling. CO2 BL3

Using waveform shown in Figure 1 for the sequential circuit given in Figure. 2, determine the flip-flop outputs (Q0,Q1,Q2,Q3) for 10 clock (CLK) pulses. Assume that all the flip-flop outputs are initialized to '1' and for the first clock pulse; the new data (input bit) is 1.

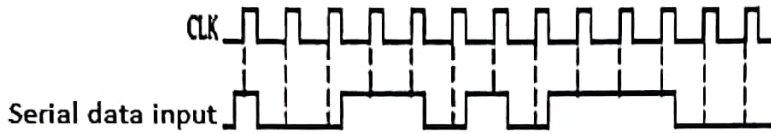


Figure 1

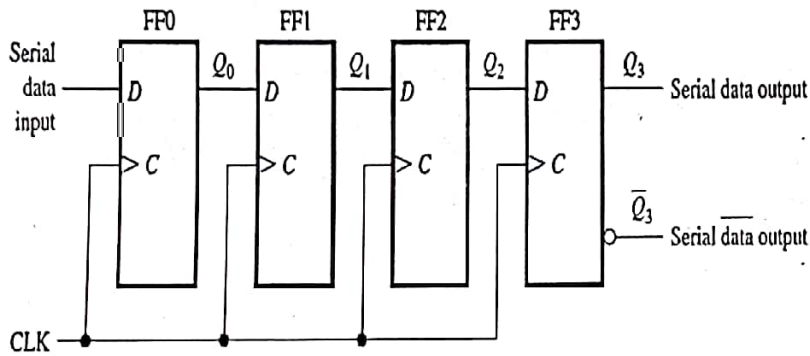


Figure 2

8.

Design a counter with the following repeated sequence 0,1,2,4, and 6 using D Flip Flop.

CO4 BL3

9.(a)

Design a Moore based finite state machine that detects the occurrence of sequence 101. The system input, output signals are given below

CO5 BL3

X	0	1	0	1	0	1	1	0	1
Y	0	0	0	1	0	1	0	0	1

OR

9.(b)

Write a behavioural verilog code for a non-overlapping mealy sequence detector that detects the sequence "1101".

CO5 BL3

10.

Implement the Boolean functions  $F(A, B, C, D) = \Sigma(1, 5, 9, 11, 12, 15)$  using programmable array logic (PAL) and programmable logical array (PLA) architectures.

CO6 BL3

↔↔↔ A/L/TY ↔↔↔