REG.NO.:

VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRICAL ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2024-2025

SLOT:B2+TB2

Programme Name & Branch	:	**B.Tech. (BEE,BEI and BEL)**
Course Code and Course Name	:	**BEEE206L- Digital Electronics**
Faculty Name(s)	:	**R.Santhakumar**
Class Number(s)	:	**VL2024250500942**
Date of Examination	:	**17/03/2025**
Exam Duration	:	**90 minutes**

Maximum Marks: 50

General instruction(s):

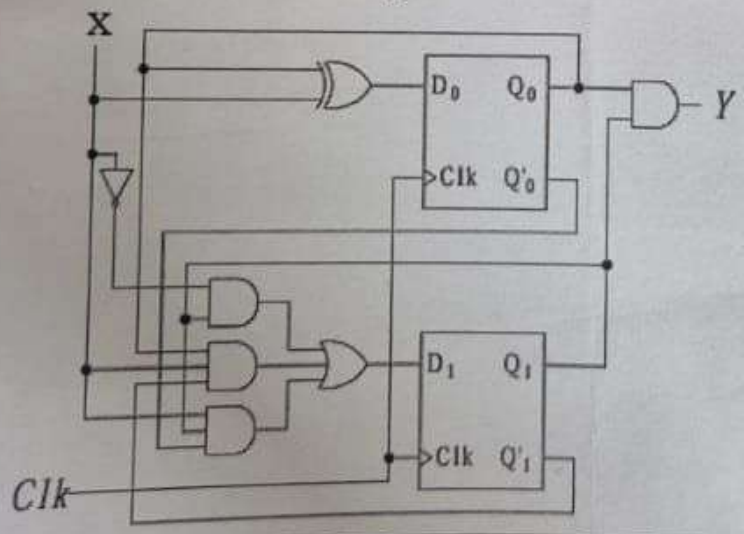
- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes Statements:

CO. 2: Design and analyze digital circuits using Verilog HDL.

CO. 3: Design and implement combinational circuits, sequential circuits and programmable logic devices.

CO. 4: Analyze and synthesize complex digital modules and circuits for various applications.

Q. No	Question	M	CO	BL
1.	Design a combinational circuit and write its equivalent Verilog HDL code and test bench code to find 2's compliment of 4-bit binary number.	10	2	2
2.	a) How to design a JK flip-flop using D flip-flop? Draw the output timing diagram of all input combination of J and K.	6	3	2
	b) How can you obtain edge triggered D flip-flop with two D flip-flop.	4		
3.	Analyse the following sequential circuit given below. The output values depend on its present state. Derive the state table with next state, output tables, and draw its state diagram. 	10	4	4
4.	Design a synchronous sequential circuit to detect the binary pattern 1101 from binary input sequence x using mealy machine non-overlapping method. Implement the circuit with T flip-flop.	10	3	2

5.	a) Draw the PAL implementation of the following Boolean function. $F1 = \Sigma(0,1,7,9,10,12,13,14,15)$.	6	4	3
	b) Implement full adder circuit with PROM.	4		