Vellore – 632014, Tamil Nadu, India

SCHOOL OF ELECTRICAL ENGINEERING

FALL SEMESTER 2023-2024

CAT-II

SLOT: F2+TF2

Programme Name & Branch : B. TECH EEE/EI Course Code: BEEE206L

Course Name : DIGITAL ELECTRONICS

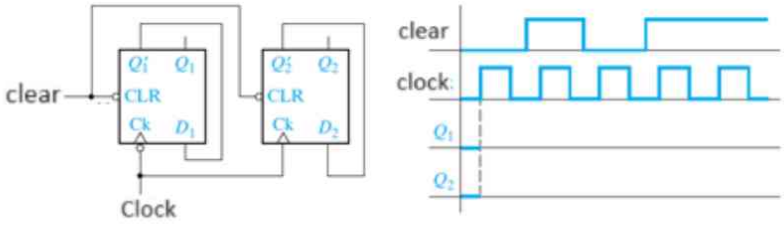
Faculty Members : Rashmi Ranjan Das, Dr. S. Balamurugan

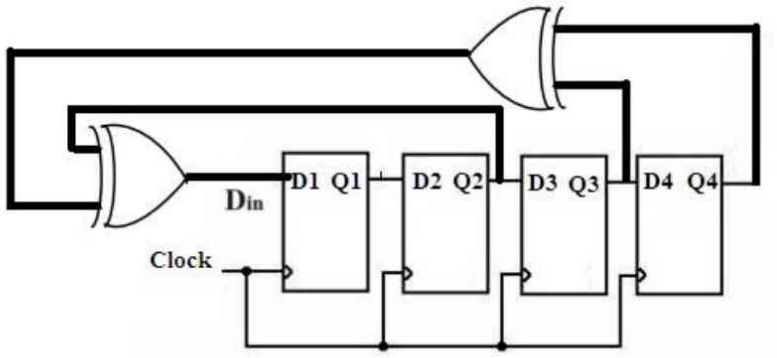
Class Number(s) : VL2023240102921/2927

Date of the Examination :20th Oct 2023

Duration: 90 minutes **Max. Marks : 50**

General instruction(s): Answer all the questions.

Q. No	Question	Marks
1.	Design a 3-bit odd parity generator circuit using NAND gates only, Write the Verilog code using Data flow modelling for the design.	10
2.	Design an Excess-3 BCD to seven segment display, Write the Verilog code for your design and the test bench code to implement the design.	10
3.	(i) Complete the timing diagram for the following circuit. Note that the clock inputs on the two flip-flops are different. [2]  (ii) An L-M flip-flop works as follows: If LM = 00, the next state of the flip-flop is 1. If LM = 01, the next state of the flip-flop is the same as the present state. If LM = 10, the next state of the flip-flop is the complement of the present state. If LM = 11, the next state of the flip-flop is 0.	10

	a) Tabulate the characteristic table. b) Derive the characteristic equation. c) Tabulate the excitation table. [8]	
4.	A sequential circuit contains a register of four flip-flops. Initially a binary number N ($0000 \leq N \leq 1100$) is stored in the flip-flops. After a single clock pulse is applied to the circuit, the register should contain $N + 0011$. In other words, the function of the sequential circuit is to add 3 to the contents of a 4bit register. Design the circuit using D-flip-flops.	10
5.	A 4-bit shift register circuit is configured for right-shift operation is D_{in} to Q_1, Q_1 to D_2, Q_2 to Q_3, Q_3 to Q_4, is shown in Figure. If the present state of the shift register is $Q_1Q_2Q_3Q_4$=0110 i. Write the truth table and timing diagram for 8 number of clock cycle. 	10