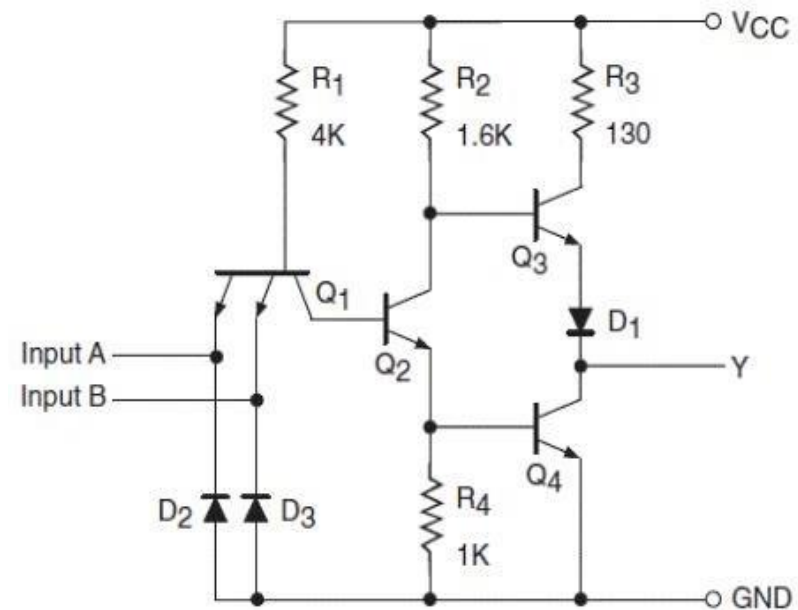


CMOS

Transistor Transistor Logic (TTL):

- It can perform many digital function and have achieved the most popularity.
- TTL IC are given the numerical designation as 5400 and 7400 series.
- The basic circuit of TTL with totem pole output stage is NAND gate.
- TTL uses a multi-emitter transistor at the input and is fast saturation logic circuit.
- The output transistor Q3 and Q4 form a totem-pole connection.
- This extra output stage is known as totem-pole stage because three output components Q3 and Q4 and Diode are stacked on one another.
- This arrangement will increase the speed of operation and also increase output current capability.
- The function of diode in this circuit prevent both Q3 and Q4 being turned ON Simultaneously.



Characteristics:

- TTL has greater speed than DTL.
- Less noise immunity.
- Power dissipation is 10mw.
- It has fan-in of 6 and fan-out of 10.
- Propagation time delay is 5-15nsec.

Name	Abbreviation	Propagation delay (ns)	Power dissipation (mw)	Speed Power Product (PJ)
Standard TTL	TTL	10	10	100
Low Power TTL	LTTL	33	1	33
High Speed TTL	HTTL	6	22	132
Schottky TTL	STTL	3	19	57
Low Power Schottky TTL	LSTTL	9.5	2	19

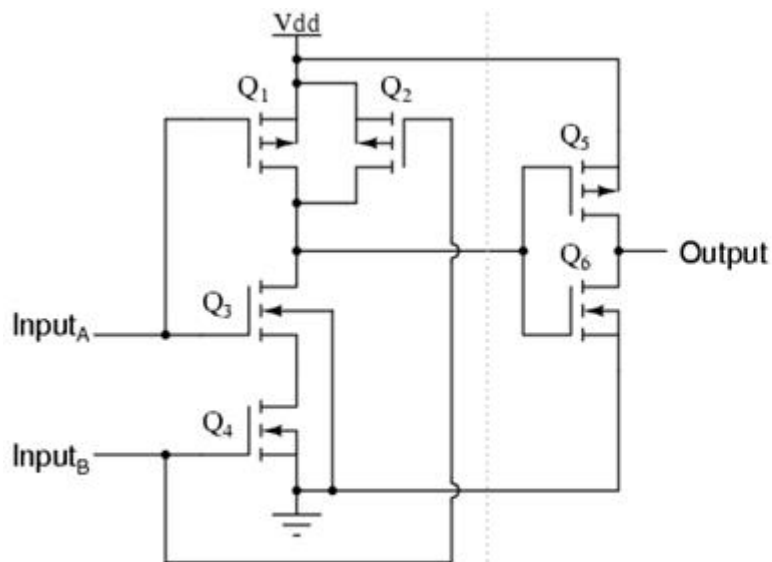
Difference between TTL and CMOS

› CMOS

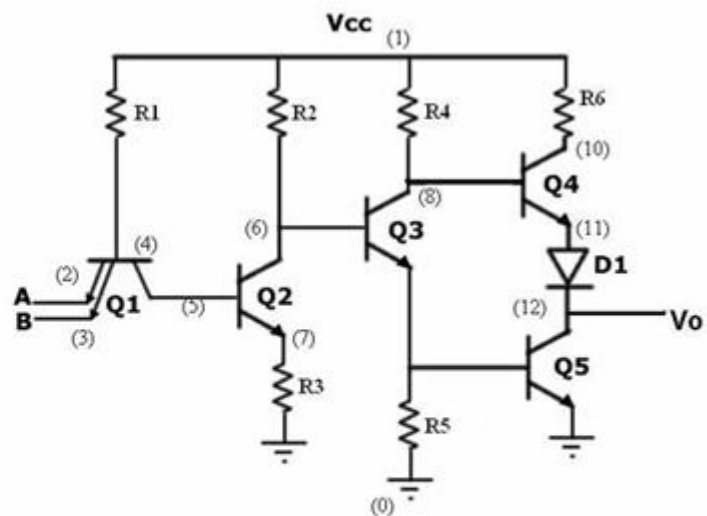
- Use FETs
- Symmetric Device Source and Drain Interchangeable
- Voltage Controlled Current Device
- Very high Input Resistance => Very low power consumption when not being used => Imperative for Small Integrated Device

› TTL

- Use BJTs
- Non Symmetric Device Non Interchangeable Collector and Emmitor
- Current Controlled Current Device
- Lower input Resistance



CMOS Logic



TTL Logic

What is a CMOS : Working Principle & Its Applications

- The term CMOS stands for “Complementary Metal Oxide Semiconductor”.
- This is one of the most popular technology in the computer chip design industry and it is broadly used today to form [integrated circuits](#) in numerous and varied applications.
- Today’s computer memories, CPUs, and cell phones make use of this technology due to several key advantages.
- This technology makes use of both P channel and N channel semiconductor devices.
- One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology.
- This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, [EEPROM and](#) application-specific integrated circuits (ASICs).

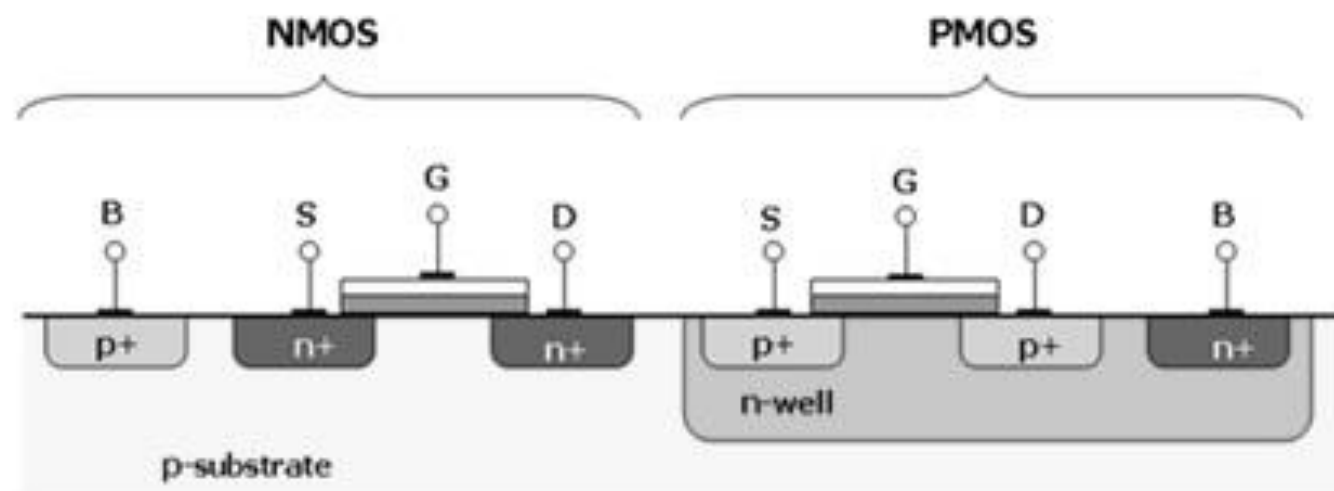
Introduction to MOS Technology

- In the IC design, the basic and most essential component is the transistor.
- So MOSFET is one kind of transistor used in many applications.
- The formation of this transistor can be done like a sandwich by including a semiconductor layer, generally a wafer, a slice from a single crystal of silicon; a layer of silicon dioxide & a metal layer.
- These layers allow the transistors to be formed within the semiconductor material. A good insulator like SiO_2 has a thin layer with a hundred molecules thickness.
- The transistors which we use polycrystalline silicon (poly) instead of metal for their gate sections.
- The Polysilicon gate of FET can be replaced almost using metal gates in large scale ICs. Sometimes, both polysilicon & metal FET's are referred to as IGFET's which means insulated gate FETs, because the SiO_2 below the gate is an insulator.

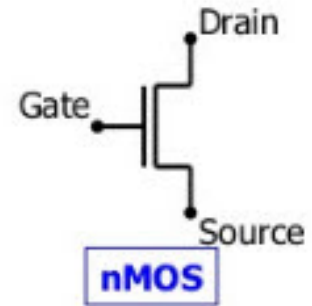
CMOS (Complementary Metal Oxide Semiconductor)

- The main [advantage of CMOS over NMOS](#) and BIPOLAR technology is the much smaller power dissipation.
- Unlike NMOS or BIPOLAR circuits, a Complementary MOS circuit has almost no static power dissipation.
- Power is only dissipated in case the circuit actually switches.
- This allows integrating more CMOS gates on an IC than in NMOS or [bipolar technology](#), resulting in much better performance.
- Complementary Metal Oxide Semiconductor transistor consists of P-channel MOS (PMOS) and N-channel MOS (NMOS).
- <https://www.elprocus.com/the-fabrication-process-of-cmos-transistor/>





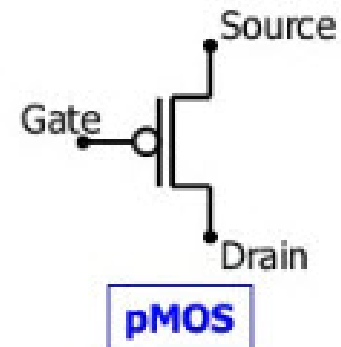
NMOS

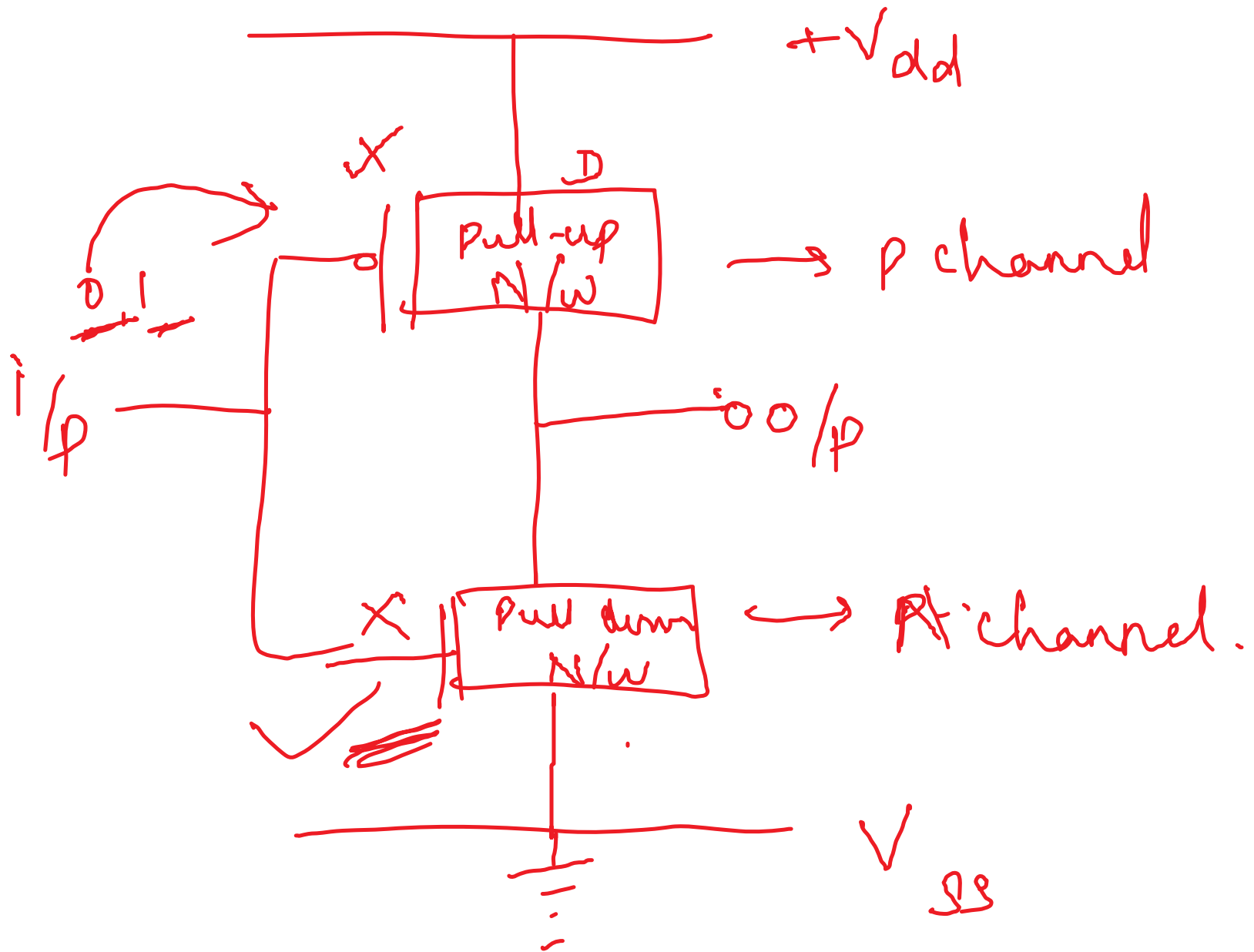


- NMOS is built on a p-type substrate with n-type source and drain diffused on it.
- In NMOS, the majority of carriers are electrons.
- When a high voltage is applied to the gate, the NMOS will conduct.
- Similarly, when a low voltage is applied to the gate, NMOS will not conduct.
- NMOS is considered to be faster than PMOS, since the carriers in NMOS, which are electrons, travel twice as fast as the holes.

PMOS

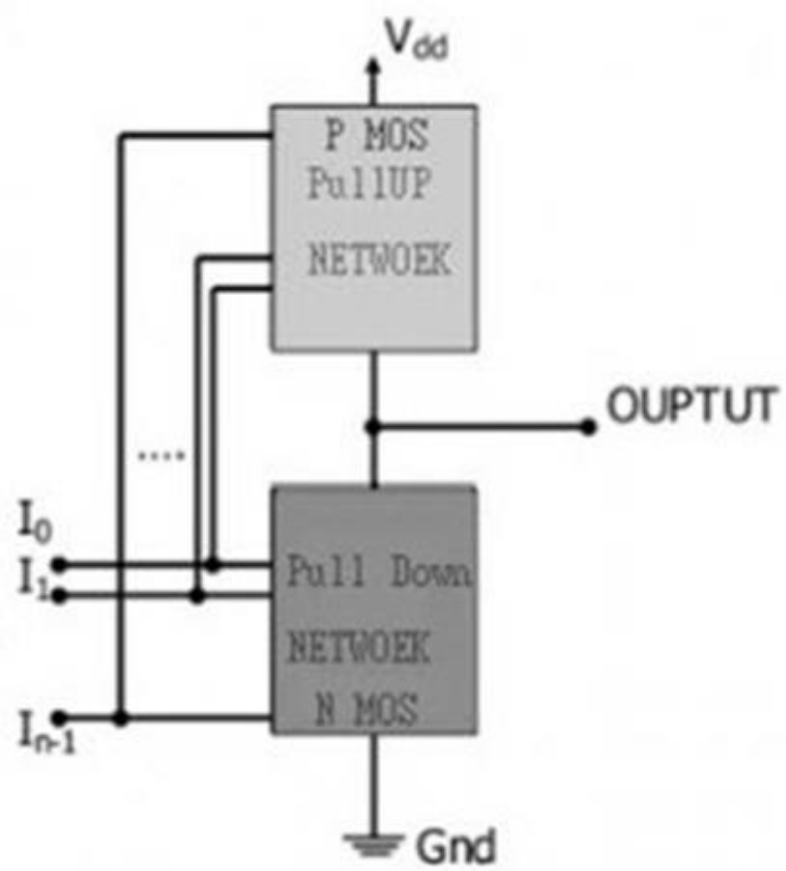
- P- channel MOSFET consists of P-type Source and Drain diffused on an N-type substrate.
- The majority of carriers are holes.
- When a high voltage is applied to the gate, the PMOS will not conduct.
- When a low voltage is applied to the gate, the PMOS will conduct.
- The PMOS devices are more immune to noise than NMOS devices.





CMOS Working Principle

- In CMOS technology, both N-type and P-type transistors are used to design logic functions.
- The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type.
- This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.
- In CMOS [logic gates](#) a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (V_{ss} or quite often ground).
- Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named V_{dd}).



CMOS

- Thus, if both a p-type and n-type transistor have their gates connected to the same input, the **p-type MOSFET will be ON when the n-type MOSFET is OFF**, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern as shown in the figure below.
- CMOS offers relatively **high speed, low power dissipation, high noise margins in both states**, and will operate over a **wide range of source and input voltages** (provided the source voltage is fixed). Furthermore, for a better understanding of the Complementary Metal Oxide Semiconductor working principle, we need to discuss in brief CMOS logic gates as explained below.

Which Devices use CMOS?

- Technology like CMOS is used in different chips like **microcontrollers, microprocessors, SRAM (static RAM) & other digital logic circuits**. This technology is used in a wide range of analog circuits which includes **data converters, image sensors & highly incorporated transceivers for several kinds of communication**.

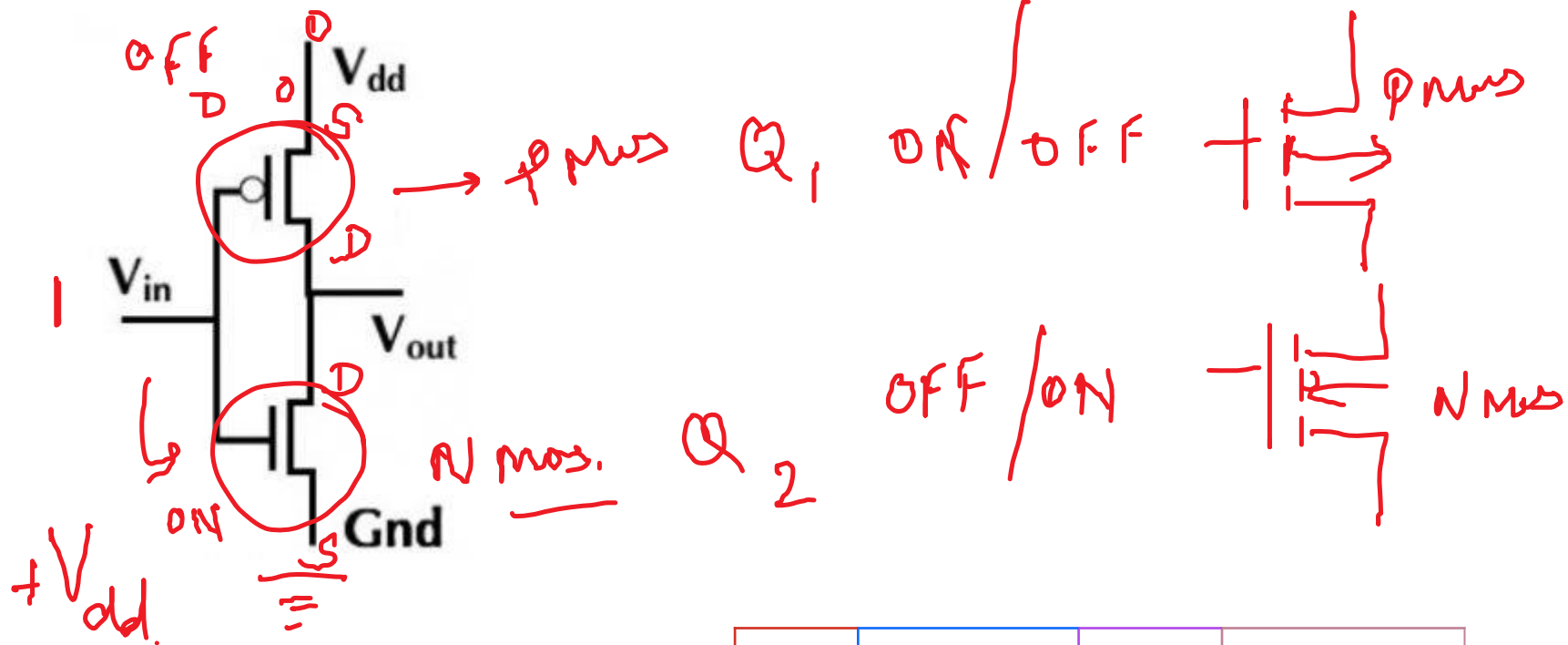
Overview

- CMOS → contains both PMOS, NMOS.
- to speed the switching of capacitive loads
- It can operated in low power
- high voltages → ^{Common} improved noise immunity

CMOS Inverter

- The inverter circuit as shown in the figure below. It consists of PMOS and NMOS FET. The input A serves as the gate voltage for both transistors.
- The **NMOS transistor has input from Vss** (ground) and the **PMOS transistor has input from Vdd**. The terminal Y is output.
- When a **high voltage ($\sim V_{dd}$)** is given at input terminal (A) of the inverter, the **PMOS becomes an open circuit**, and NMOS switched OFF so the output will be pulled down to Vss.

CMOS Inverter

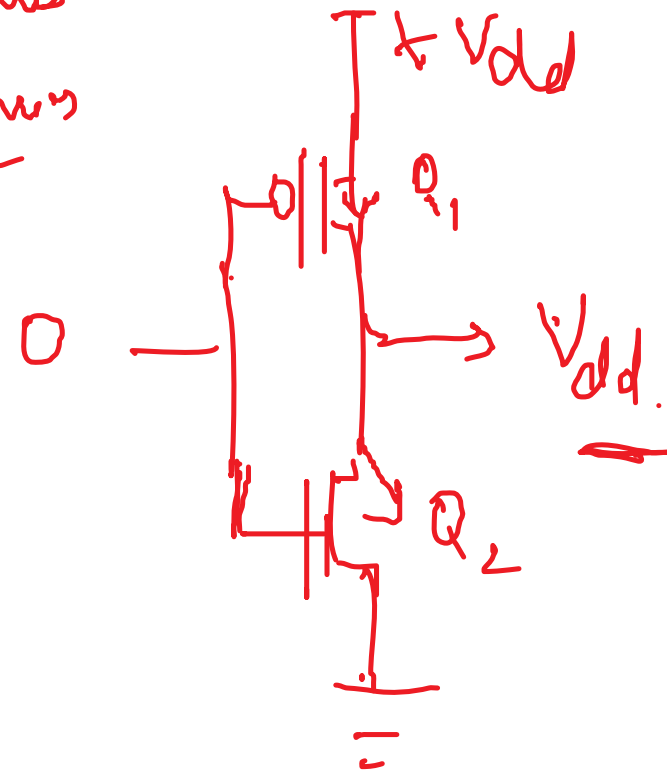
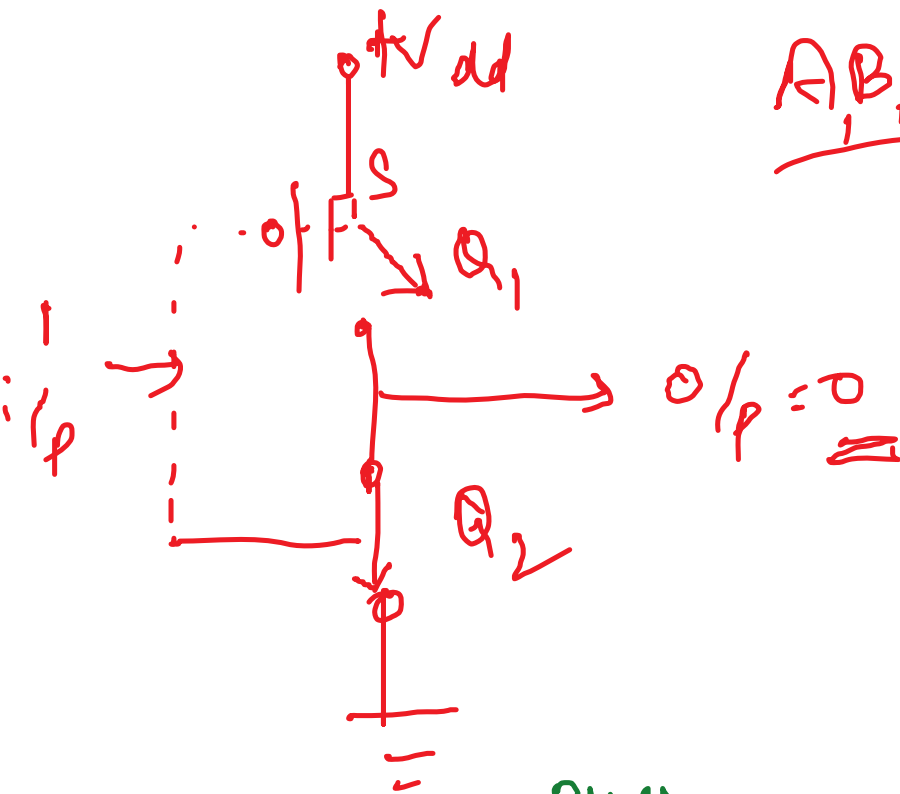


When a low-level voltage ($<V_{dd}$, $\sim 0V$) applied to the inverter, the NMOS switched OFF and PMOS switched ON. So the output becomes V_{dd} or the circuit is pulled up to V_{dd} .

INP UT	LOGIC INPUT	OUTP UT	LOGIC OUTPUT
0 v	0	V_{dd}	1
V_{dd}	1	0 v	0

Q_2

ABC ③ → PMOS
 ③ → NMOS



	PMOS	NMOS	O/p
A	Q ₁	Q ₂	
0	ON	OFF	↑ (V _{dd})
1	OFF	ON	0

Not

0 1

2-1/2 NAND $\rightarrow$ AND + NOT

CMOS NAND



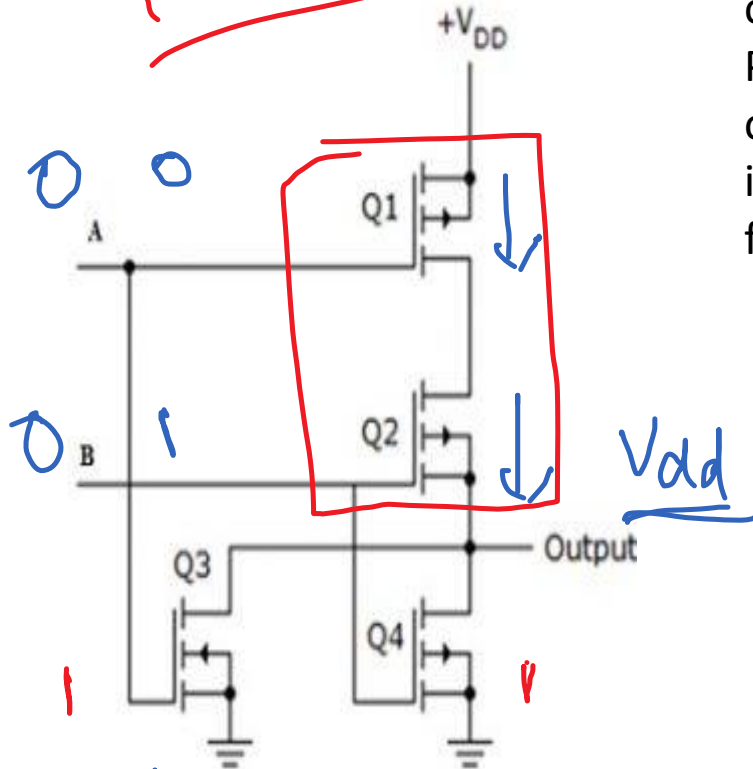
If either input A or B is logic 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to Ground. But at least one of the pMOS transistors will be ON, creating a path from Y to VDD.

Hence, the output Y will be high. If both inputs are high, both of the nMOS transistors will be ON and both of the pMOS transistors will be OFF. Hence, the output will be logic low. The truth table of the NAND logic gate given in the below table.

$$p_{max} \geq 0/p$$

CMOS NOR Gate

The NMOS transistors are in parallel to pull the output low when either input is high. The PMOS transistors are in series to pull the output high when both inputs are low, as given in the below table. The output is never left floating.



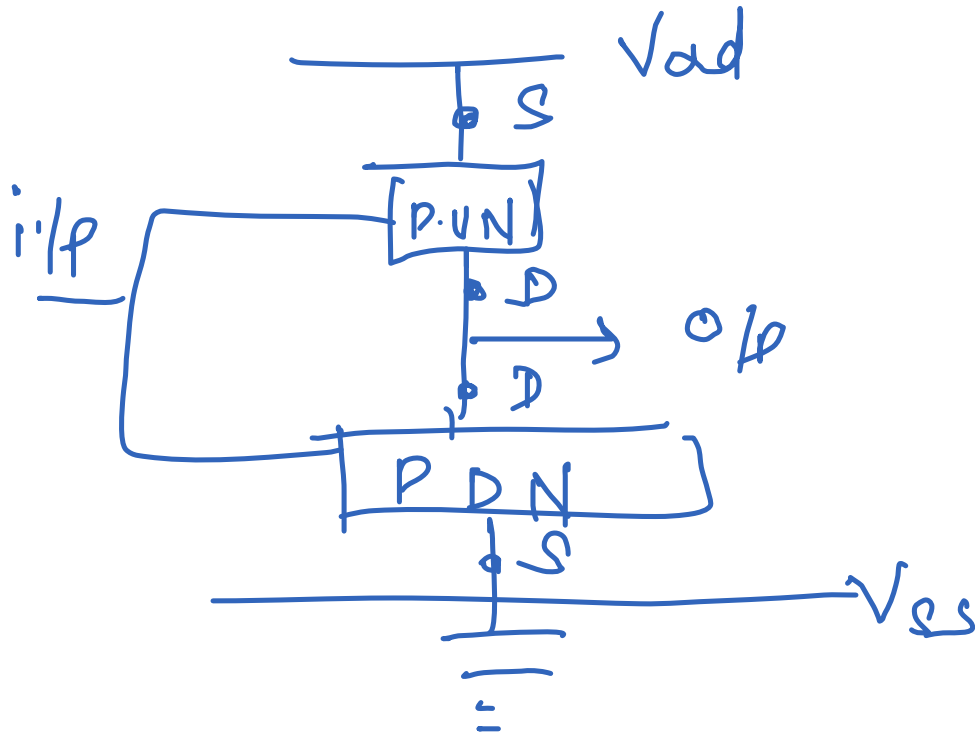
The truth table of the NOR logic gate given in the below table.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NMOS $\rightarrow$ sein
PMOS $\rightarrow$ 11^{er}

KMOS $\rightarrow$ 11^{er}
PMOS $\rightarrow$ sein.

$$F = (A + B + C)D$$



$A, B, C, D \Rightarrow 4$ transistors
 $4 \rightarrow$ PMOS
 $4 \rightarrow$ NMOS

$$F = \underbrace{A \cdot B}_{\text{Series}} \text{ NMOS}$$

$$F = \left. \begin{array}{l} A + B \\ \text{||} \end{array} \right\} \rightarrow \text{PMOS}$$

$$\sqrt{F}: A + B \rightarrow \text{NMOS}$$

$$F: A + B \rightarrow \text{Series} \rightarrow \text{PMOS}$$