REG.NO.: 26BEC0497

# VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
FALL SEMESTER 2026-2027

SLOT: C1+TC1+TCC1

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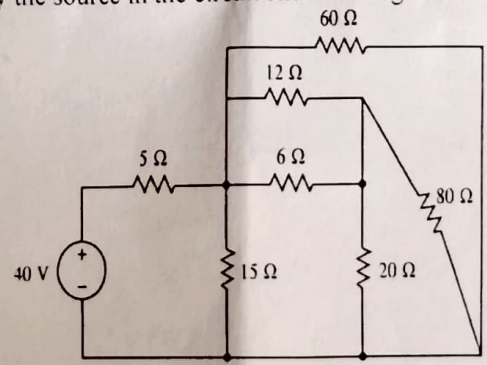
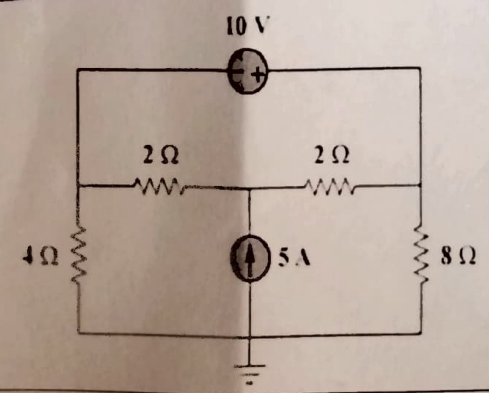
| Programme Name & Branch | : B.Tech ECE, BVD, BLC |
| Course Code and Course Name | : BAECE103 & Network Theory |
| Faculty Name(s) | : DHARANI BAI G, VIJAY KUMAR, NITHISH KUMAR V, NAVEEN MISHRA, SHANIDUL HOQUE, MOHIUL ISLAM, HENRIDASS, SUDIPTA KUMAR SARKAR |
| Class Number(s) | : VL2026270105286/5293/5313/5291/5296/5299/5315/5288 |
| Date of Examination | : 11.08.2026 |
| Exam Duration | : 90 minutes (9.30 AM – 11.00 AM) Maximum Marks: 50 |

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level
  (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

**Course Outcomes are:**

1. Compute DC circuit parameters using circuit laws and theorems
2. Determine the natural and step responses of RC, RL, and RLC circuits
3. Apply appropriate techniques and theorems for sinusoidal steady-state analysis
4. Apply the Laplace transform to circuits for steady-state and transient analysis
5. Compute two-port network parameters and network graph matrices for circuit analysis

| Q. No. | Question | CO | BL | Marks |
|---|---|---|---|---|
| 1. | Apply appropriate circuit reduction techniques to determine the equivalent resistance seen by the source in the circuit shown in Figure 1.   Figure 1 | 1 | BL3 | 10 |
| 2. | Calculate all the node voltages in the circuit shown in Figure 2 using nodal analysis   | 1 | BL3 | 10 |

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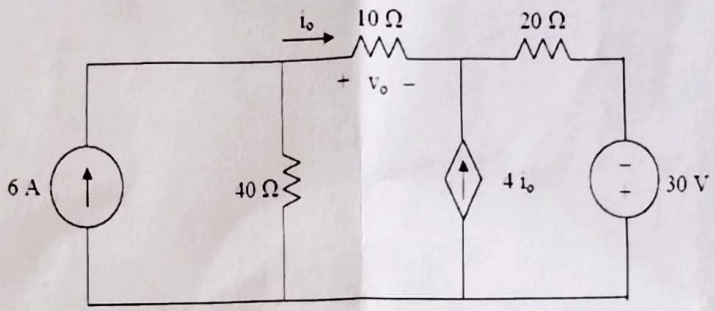
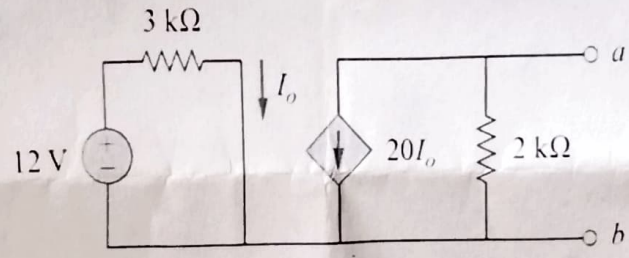
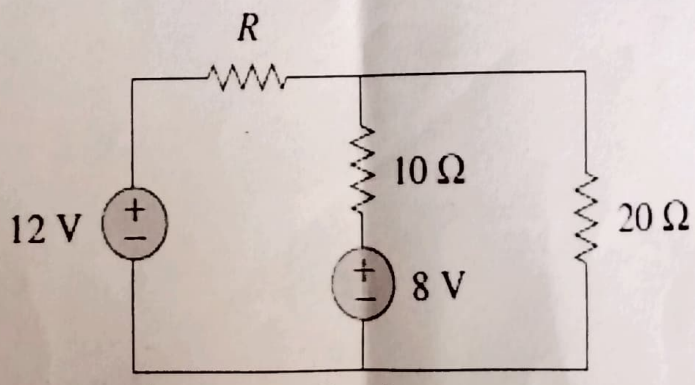
|---|---|---|---|---|
| | Figure 2 | | | |
| 3. | Use the superposition principle to find $i_o$ in the circuit shown in Figure 3.   Figure 3 | 1 | BL3 | 10 |
| 4. | Find the Thevenin equivalent circuit between terminals *a-b* of the circuit shown in Figure 4.   Figure 4 | 1 | BL3 | 10 |
| 5. | Compute the value of R that results in maximum power transfer to the 10 Ω resistor in the circuit shown in Figure 5.   Figure 5 | 1 | BL3 | 10 |

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