VIT
Vellore Institute of Technology

School of Electronics Engineering

Winter Semester 2022-23 Continuous Assessment Test – I

Program Name & Branch: B.Tech (School of Computer Science Engineering) **SLOT: C2+TC2**
Course Name & Code: Microprocessors and Microcontrollers BECE204L
Exam Duration: 90 Min. **Maximum Marks: 50**

Q. No.	Questions	Max Marks	CO	BL
1.	a) Identify the addressing mode for 1) POP 0 2) MOV A, #255 3) MUL AB 4) MOV 40H, #40H 5) MOV @R1, A b) Summarize bits of PSW bit in 8051 microcontroller. Give a sequence of instruction to switch from bank 0 to bank 2.	10 (5+5)	CO1	BL1
2.	a) Sketch the content of the stack after the execution of the following code: **PC Opcode Mnemonic Operand** 000B 120300 LCALL DELAY 000E 80F0 SJMP BACK 0010 ; ----------this is the delay subroutine 0300 ORG 300H 0300 DELAY: 0300 7DFF MOV R5, #0FFH 0302 DDFE AGAIN: DJNZ R5, AGAIN 0304 22 RET b) After reset, the contents of internal memory of 8051 microcontroller with address 0AH and 0BH contains data 22H and 33H, respectively. Sketch the contents of internal memory from address 07H to 0BH and the content of the register and SP, after executing the following code: PUSH 0AH PUSH 0BH POP 09H	10	CO 3	BL3
3.	Write an ALP in 8051 microcontroller to load the first 10 even numbers within the range of 1-20 in RAM locations starting at 35H. Calculate their sum and store the result in 40h.	10	CO 3	BL4

4.	Determine the value of register A, register B and status of the flag register by considering step by step execution of the following instructions:
	
	ORG 0000H
	MOV A, #25H
	MOV B, #1FH
	MUL AB
	SUBB A, #0FCH
	RRC A
	END
		10	CO 3	BL5

5.	If the XTAL frequency of 8051 is 12 MHz, examine the time taken to execute the following program. The machine cycle for each instruction is mentioned in the parenthesis,	10	CO 3	BL4

	OPCODE/OPERAND	MACHINE CYCLE
	MOV R5, #2	1
HERE 1:	MOV R4, #180	1
HERE 2:	MOV R3, #255	1
HERE 3:	DJNZ R3, HERE3	2
	DJNZ R4, HERE2	2
	DJNZ R5, HERE1	2
	RET	2

1652403 µs