W/D/TY

Reg. No: 23BCE0109

VIT®
Vellore Institute of Technology

Final Assessment Test – April 2025

Course: BECE204L - Microprocessors and Microcontrollers

Class/ NBR(s): 4038 / 4040 / 4042 / 4045 / 4047 / 4049 / 4051 / 4054 / 4057 / 4059 / 4061 / 4063 / 4065 / 4068 / 4071 / 4073 / 4075 / 4077 / 4078 / 4080 / 4082 / 4084 / 4086 / 4088 / 4191 / 4199 Slot: B1+TB1

Time: Three Hours Max. Marks:

- KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPR
- DON'T WRITE ANYTHING ON THE QUESTION PAPER

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Explain the concept of interrupt handling in an 8-bit embedded system. How does the processor manage multiple interrupts, and what is the significance of interrupt prioritization in embedded systems?

2. (i) The 8086 microprocessor has a 16-bit data bus and a 20-bit address bus. How does this affect the addressing capability, and what limitations does this impose on memory access?

   (ii) In 8086 Microprocessor, demonstrate the content of FLAGS after performing $(FFFF)_{16} + (0001)_{16}$

3. Develop an 8051 Assembly Language Program (ALP) to count the number of high bits (1s) of 8 bit data stored at RAM location 30H. Store the count in 31H.

4. For the following 8051 ALP, list the sequences of actions taking place while executing the entire program. Demonstrate your answer using proper sketch of Program Counter.

ROM LOCATION	INSTRUCTION
0000H	ORG 0000H
0001H	START:
0002H	MOV SP, #70H
0004H	MOV R0, #05
0005H	MOV R1, #00
0006H	LCALL CALC_SUM
0009H	HERE: SJMP HERE
0100H	CALC_SUM:
0101H	MOV A, R1
0102H	ADD A, R0
0103H	MOV R1,A
0104H	DJNZ R0, CALC_SUM
0106H	MOV B, R1
0107H	RET

5. Develop an 8051 ALP in which 8051 gets data from P1 and sends it to P2 continuously while incoming data from the serial port is sent to P0. Assume that XTAL=11.0592 MHz. Set the baud rate at 9600.

6. Assume there are two switches connected to MSB and LSB pins of Port 0 of 8051 Microcontroller. Develop an ALP that continuously monitors the MSB and LSB pins of P0 and based on the binary combinations; perform the actions as given in table 1.

Table1

S.No	MSB	LSB	Action
1	0	1	Generate a waveform of frequency 5KHz at P1.0 use Timer 0
2	1	0	Transmit character "A" continuously at the baud rate of 19200

7.(a) Develop an 8051 assembly code to display the string "HELLO" on a common cathode 7-segment display with a 500ms interval between each character. Assume that the pattern for "H", "E", "L", "L", "O" are stored in ROM starting at 400H. Use Timer 1 to generate 500ms of delay.

OR

7.(b) Develop an 8051 ALP to display a sequence of numbers on a 16x2 LCD. Assume the numbers (e.g., "1", "2", "3", ...till "9") are stored in ROM starting at 800H as ASCII values. The program should display these numbers sequentially on the first row of the LCD, with each number appearing for 1 second before the next number is displayed. Use Timer 0 to generate the delay.

Reference:

01 – clear display
38 – 2 lines 5X7 matrix
0E – Display ON cursor blinking
06 – Increment cursor
04 – Decrement cursor
80 – Force cursor to beginning of first line.
C0 - force cursor to beginning of Second line

8.(a) Draw the diagram for interfacing 8051 with DAC 0808 at Port P1. Develop 8051 assembly programs to generate (i) a stair-step ramp waveform and (ii) a triangular waveform.

OR

8.(b) Assume a pH sensor is used to measure the soil pH level and is interfaced with an 8051 microcontroller. Design the block diagram and a circuit diagram for the interfacing. The sensor provides an analog output corresponding to the pH value. Assume step size of 10mV. Explain the necessary signal conditioning and how the 8051 processes the sensor's data to display the pH level.

9. (i) The ARM core follows the RISC (Reduced Instruction Set Computing) architecture, which emphasizes delivering simple yet efficient instructions. How do the four key design principles of RISC architecture contribute to its performance in real-time applications, such as smartphones or embedded systems?

(ii) Describe the different processor modes in ARM processors and explain the corresponding register banks associated with each mode. Use diagrams to illustrate how these modes operate, highlighting how each mode facilitates efficient processing and system management.

10. (i) Explain with examples the different addressing modes for single register load-store ARM instructions.

(ii) Explain the effect of barrel shifter on the following instructions in an ARM processor. What is the result of the Logical Shift Left operation on these instructions?

(a) MOV r7, r5, LSL #2

(b) ADD r0, r1, r1 LSL #1

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