E/L/TX

Final Assessment Test – November 2024

Course: **BECE102L - Digital Systems Design**

Class NBR(s): **4252 / 4256 / 4262 / 4264 / 4266 / 4269 / 4271 / 4273 / 4276 / 4278 / 4280 / 4284 / 4287 / 4292 / 4293 / 4297 / 4299 / 4310 / 4311**

Slot: **E1+TE1**

Time: **Three Hours**

Max. Marks: **100**

- **KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Simplify the following using Boolean Algebra and draw the circuit using CMOS logic.

$$F = [A\overline{B}(C + BD) + \overline{AB}]C$$

2. i) Simplify the following to POS using K – Map. **[5]**

Y (A, B, C, D) = ∑m(1,5,7,9,13,14) + d(2,4,10,11,12,15)

ii) Redraw the following circuit shown in Figure 1 using only NAND gates without losing the functionality. **[5]**

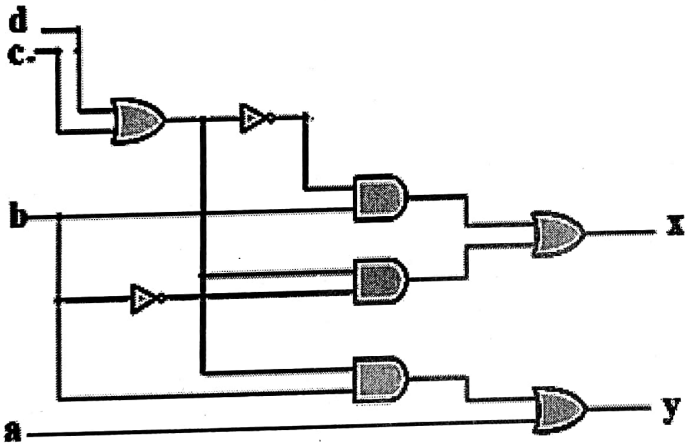


Figure 1

3. Derive the truth table and draw the circuit for the below Verilog HDL code

```
module fat3(in,out);
        input [2:0]in;
        output [2:0]out;
        reg [2:0]out;
        always @ (in)
          begin
            case (in)
              0 : out = 0;
```

```
        1 : out = 1;
        2 : out = 3;
        3 : out = 2;
        4 : out = 6;
        5 : out = 7;
        6 : out = 5;
        7 : out = 4;
    endcase
end
endmodule
```

4. **Scenario**: Design a traffic light control system for a two-way intersection, where each direction has a red, yellow, and green light.

Inputs:

- **A**: Sensor for Direction 1 (1 if a vehicle is present, 0 otherwise)
- **B**: Sensor for Direction 2 (1 if a vehicle is present, 0 otherwise)
- **C**: Emergency Vehicle Signal (1 if an emergency vehicle is approaching, 0 otherwise)

Tasks:

i. **Design a truth table** for the traffic light system, specifying the output signals for each light (R1, G1, Y1 for Direction 1 and R2, G2, Y2 for Direction 2).

ii. **Derive the logic expressions** for each output using AND, OR, and NOT gates based on the truth table.

iii. **Implement the logic expressions** using basic gates and draw the circuit diagram.

iv. Write the gate level HDL.

5. Design the full adder using PAL and write down the logical expression of Adder.

6. Design a circuit that compares two binary numbers X and Y, each having two bits ($X = X_2 X_1$; $Y = Y_1 Y_2$). It has two outputs A and C.

(i) A is supposed to be 1 when $X > Y$

(ii) C is 1 when $X = Y$.

Do not use adders/subtractor for this design; instead use a fundamental design process. Draw the minimum sum-of-products circuit. Assume complemented inputs are NOT available, but multiple input gates can be considered.

7. (ii) Construct a state table for the circuit shown in Figure 2. Obtain the equation for the next value of the output Q in terms of Q, A and B. write the dataflow HDL. [5]

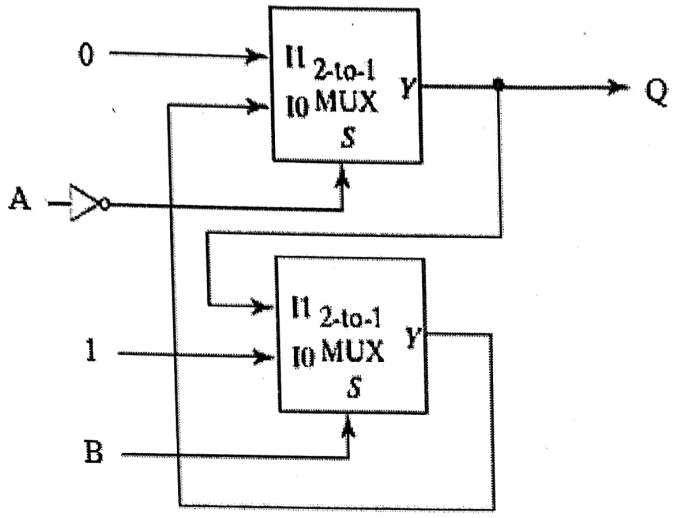


Figure 2

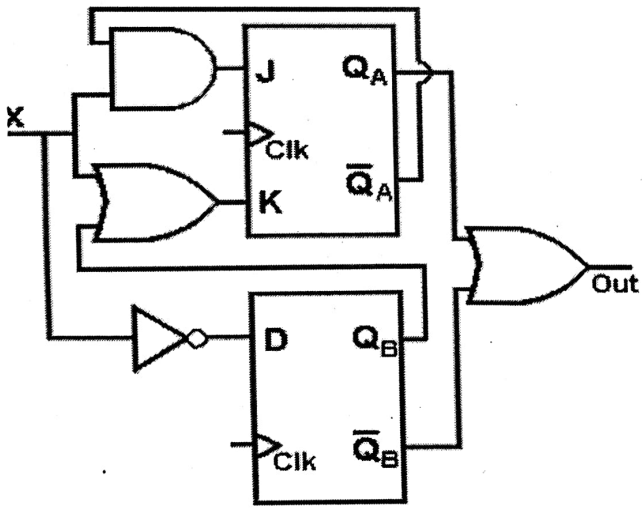
(ii) Convert D- Flip Flop to T – Flip Flop. [5]

8. Design a synchronous MOD-12 counter using D - FF. Write behavioral Verilog code and the test bench to verify the design.

9.(a) Design a Moore Sequential Circuit whose output is 1, whenever the input sequence ends with 1001. Design the circuit using JK – FF.

OR

9.(b) Analyse the given circuit and draw the state diagram and state table



10.(a) Implement the following function using only one 4:1 Digital Switch and external logic gates. Where P and R are selection lines.

$$F\,(PQRS) = P\bar{Q}\,\bar{R} + \bar{P}\,QR + PQRS + \overline{(Q+R+S)}$$

OR

10.(b) Design a circuit using Decoder to convert 8421 code to Gray code.

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