VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT: A1 +TA1

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

Programme Name & Branch	**: BCE, BAI, BCB, BCI, BCT, BCT, BDS, BKT, BME, BEL, BYB**
Course Code and Course Name	**: BCSE205L and Computer Architecture and Organization**
Faculty Name(s)	**: Common to all classes**
Class Number(s)	**: VL2025260501998, 1988, 1903, 2001, 1866, 1985, 1870, 1953, 1898, 4005, 1901, 2024, 5391, 1880, 3865, 1896, 2022, 2006, 1968, 1873**
Date of Examination	**: 27/01/2026**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes:
  CO1: Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.

Q. No	Question	Module	Marks	CO	BL
1.	Explain the architecture of the IAS computer with the help of a neat block diagram. Using the instruction sequence, X=A/B, illustrate the flow of data and control information through the IAS registers during the execution of this instruction sequence.	1	10	CO1	BL1
2.	Apply the non-restoring division algorithm to divide 18 by 6, showing the contents of the accumulator and quotient register at each iteration. Explain the operational flow of the non-restoring division using a suitable flowchart.	2	10	CO1	BL3
3.	a) Using Modified Booth's algorithm, find the product of –21 × 5.	2	7	CO1	BL3
	b) Highlight the advantages of Modified Booth's algorithm over conventional Booth multiplication	2	3		
4.	Consider a processor with the following initial system state: • Instruction stored at memory location 300 • Address field stored at location 301 with a value of 600 • Index register R1 = 200 a) Calculate the effective address for (4 marks) • Direct addressing mode • Indirect addressing mode • Auto increment addressing mode • Immediate addressing mode	3	10	CO1	BL3

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT: A1 +TA1

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

	b) Analyze how relative addressing and indexed addressing compute the effective address using the given system state. (2 marks) c) Suppose the program is relocated and the instruction moves from memory location 300 to 1300. Recompute the effective address for both addressing modes. Evaluate the impact of program relocation on relative and indexed addressing mode and justify your answer. (4 marks)				
5.	a) Compare RISC and CISC.	1	5	CO1	BL3
	b) Assume a computer system in which both address and data fields are 24 bits wide, and the word length is 8 bits. I. Analyze how the expression $X = (A - B) \times C$ is evaluated using one-address instruction format and two address instruction formats. II. Determine the number of memory accesses (memory traffic) involved.	3	5		

****