VIT
Vellore Institute of Technology

Final Assessment Test – November 2022

Course: BECE102L - Digital Systems Design
Class NBR(s): 4423/4432/4436/4440/4442/4444/ 4445/4447/4573/4575
Slot: D2+TD2

Time: Three Hours
Max. Marks: 100

KEEPING MOBILE PHONE/SMART WATCH, EVEN IN 'OFF' POSITION, IS TREATED AS EXAM MALPRACTICE

Answer ALL Questions

(10 X 10 = 100 Marks)

1. Simplify the following Boolean expression to standard SoP and standard PoS. Implement the following simplified Boolean expressions using NAND gate and NOR gate circuits.

   $F(A,B,C,D) = \sum m (5, 6, 7, 8, 11)$.

2. i) Implement the simplified expression of the Boolean function $F(w, x, y, z) = \sum m (0, 1, 4, 8, 9, 10) + \sum d (2, 11)$ using basic gates. [5]

   ii) Simplify $F(x,y,z) = xy + xy'(x'z')'$ with Boolean algebra properties. [5]

3. a) Draw the block diagram of 16 X 1 Multiplexer using 4 X 1 multiplexers. Write Verilog HDL for a 4 X 1 multiplexer using case statement. Write a structural Verilog code for a 16 X 1 Mux using 4 X 1 mux.

[OR]

3. b) Using continuous assignments, write a Verilog description of the circuit specified by the following Boolean functions and its test bench:

$$Out\_1 = (A + B')C'(C + D)$$
$$Out\_2 = (C'D + BCD + CD')(A' + B)$$
$$Out\_3 = (AB + C)D + B'C$$

   Also draw the combined block diagram of the above function using logic gates.

4. Implement the following Boolean function $F(A,B,C,D) = \sum m (1, 3, 5, 10, 12)$. Using 4 to 1 multiplexer and 2 to 1 multiplexer. No other logic gate is allowed except NOT gate.

5. Implement the following Boolean function

   $F(A,B,C,D) = \sum m (2, 4, 9, 14, 15)$. Using

   i) 1 to 16 demultiplexer [5]

   ii) 4:16 decoder. [5]

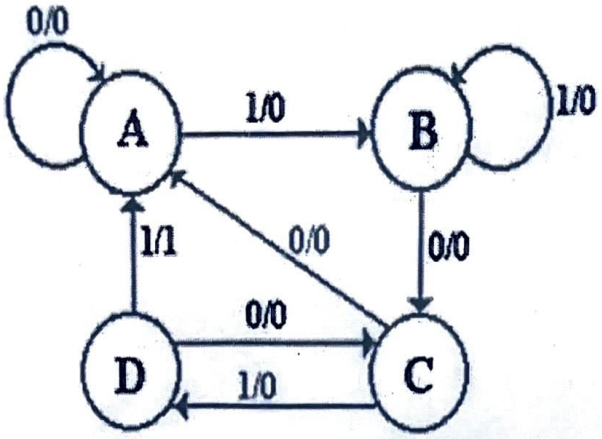
6. Calculate the product of 4-bit signed numbers 0011 and 1100 using booth's algorithm and describe the architecture of booth multiplier.

7. a) Design a 4-bit counter that counts from 0 to 10 using D-flipflop and provide necessary circuit diagram.

[OR]

7. b) Design a circuit for a positive edge triggered 4-bit binary up counter (0000 to 1111). When it reaches "1111", it should revert back to "0000" after the next edge. Use positive edge triggered D flip-flop to design the circuit.

8. Design the sequential circuit for the following state diagram using JK-flipflop.



9. Design a sequential circuit to detect the sequence 101 (without overlapping) using D-flip flop.

10. Compare and contrast the architectures of PAL, PLA and FPGA with diagrams.

⇔⇔⇔