VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

School of Electronics Engineering

WEI_2022-23 (CAT-I)

Course Code	:	**BECE102L**	**Duration : 90 Minutes.**
Course Name	:	**Digital Systems Design**	
Class Numbers	:	**VL2022230506857**	
Faculty Name	:	**Dr. Abhishek N. Tripathi**	
Slot	:	**X11+X12+X21**	**Max. Marks : 50M**

Answer all the questions

S. No.	Questions	Mark
1	(i) By Boolean algebra prove that the Boolean function F = A + A'B + A'B'C + A'B'C'D = A+B+C+D (ii) Obtain the canonical POS of the expression F = AB + A'C	5 5
2	Obtain the a) minimum POS and (b) minimum SOP of the following function $F(A,B,C,D) = \Sigma m(2,3,6,7,12,13,14)$	10
3	Realize the function using (a) NAND logic (b) NOR logic F(A,B,C,D) = (A'B' + AB) (CD' + C'D)	10
4	Design a Full adder circuit using two half adders and write a gate level modelling program for the designed full adder.	10
5	(i) Draw the logic diagram of the digital circuit specified by the following Verilog description **module Circuit_C (y1, y2, y3, a, b);** **output y1, y2, y3;** **input a, b;** **assign y1 = a || b;** **and (y2, !a, b);** **assign y3 = a && (!b);** **endmodule**	5
	(ii) Consider the following inputs to solve the expressions. **a=3'110 , b=3'0xx ,c=3'0x1 , d=3'0zz, e= 3'101** **f1= (a^b)** **f2=(a & b)** **f3={3{a,2{b},11}}** **f4=(a!=c)** **f5=(c===d)**	5