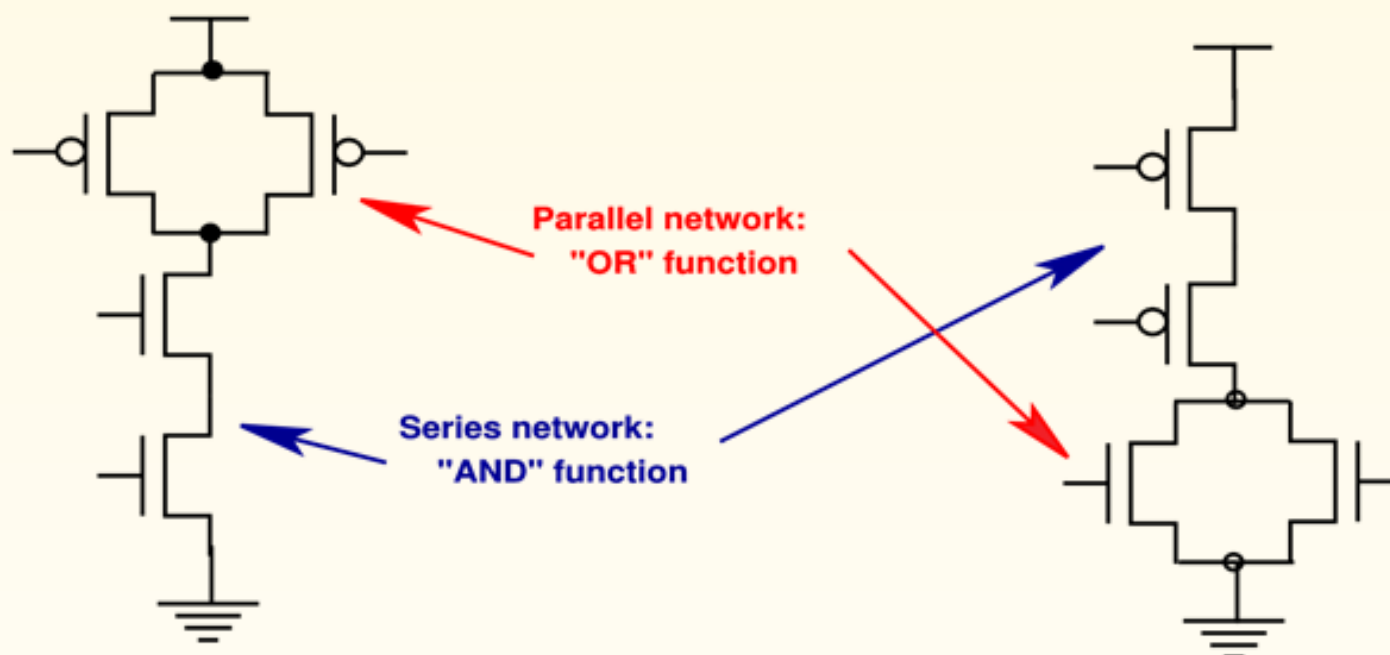


CMOS Design and Implementation

Static CMOS Circuits

N- and P-channel Networks

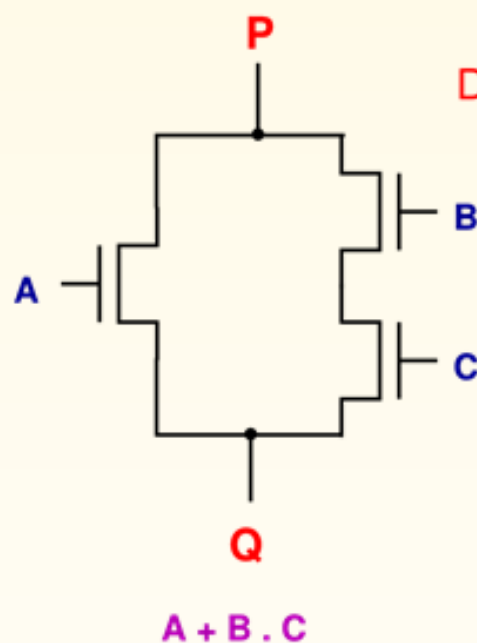
- N- and P-channel networks implement logic functions
 - Each network connected between **Output** and V_{DD} or V_{SS}
 - Function defines path between the terminals



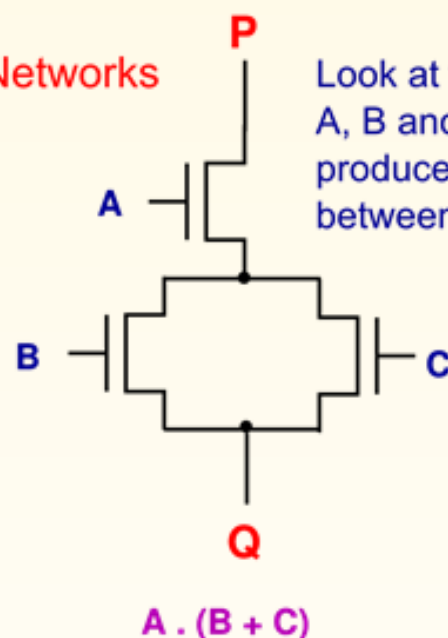
Duality in CMOS Networks

Straightforward way of constructing static CMOS circuits is to implement dual N- and P- networks

- N- and P- networks must implement **complementary** functions
- Duality **sufficient** for correct operation (but not necessary)



Dual Networks

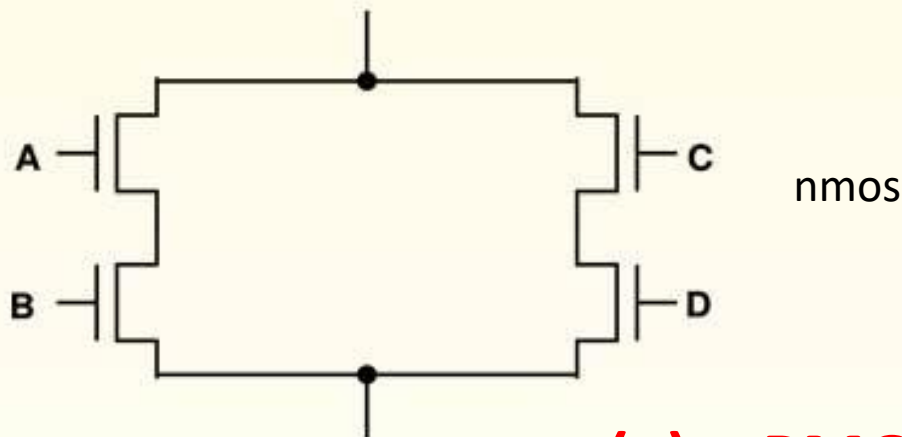


Look at functions of A, B and C, which will produce a connection between P and Q

Constructing Complex Gates

Example: $F = \overline{(A \ B) + (C \ D)}$

- 1 Take uninverted function $F = (A \ B) + (C \ D)$ and derive N-network
- 2 Identify *AND*, *OR* components: F is *OR* of AB , CD
- 3 Make connections of transistors



(.) – NMOS –series
PMOS- Parallel

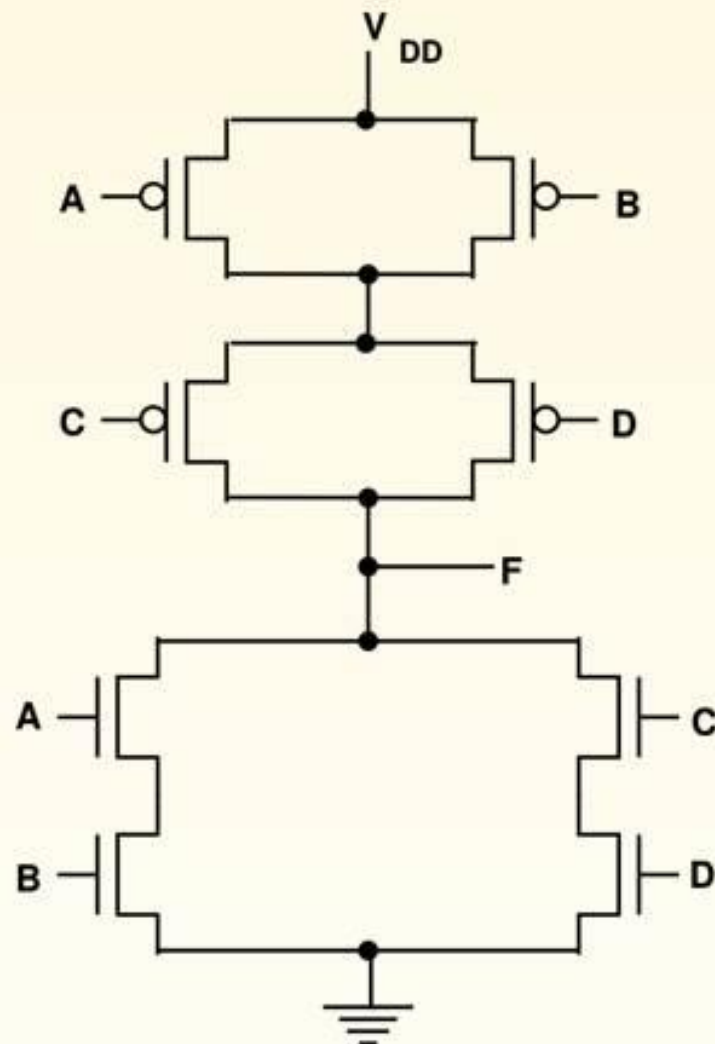
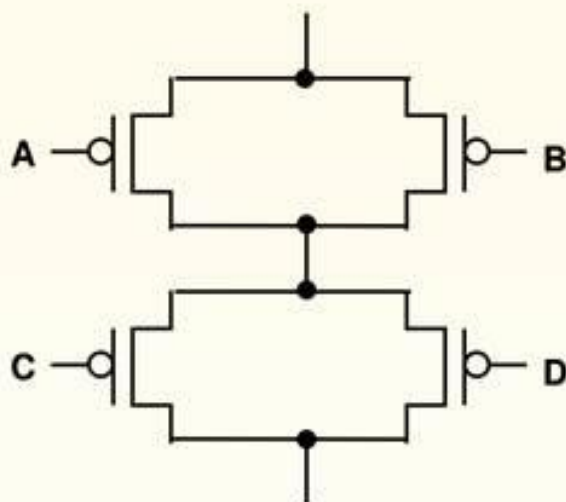
(+) – PMOS –series
NMOS- Parallel

Construction of Complex Gates, Cont'd

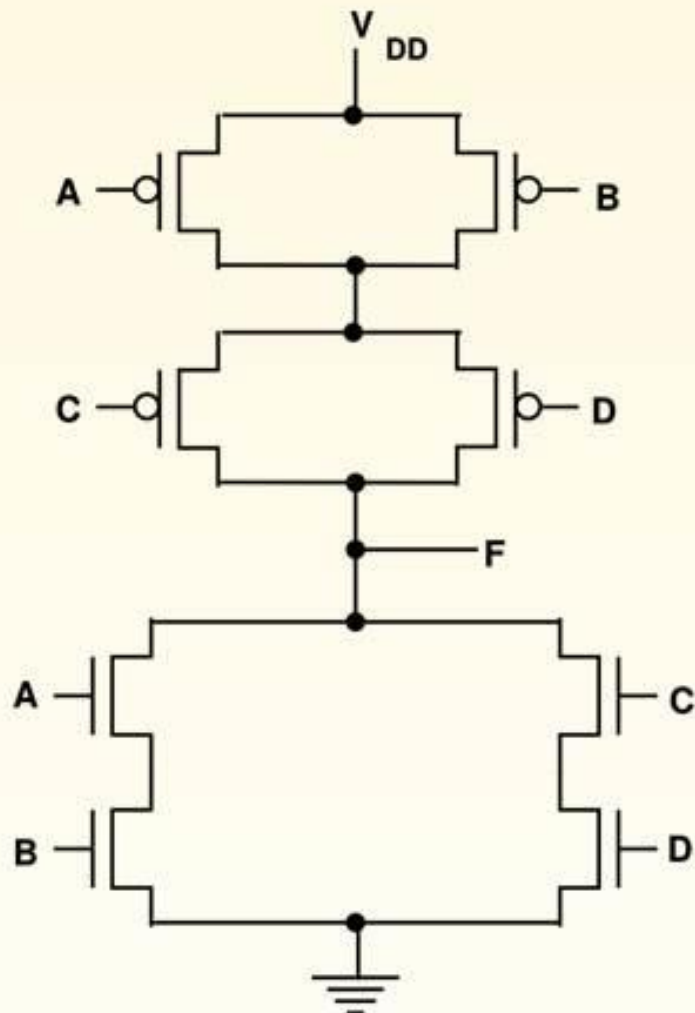
- 4 Construct P-network by taking complement of N-expression $(A B + C D)$, which gives the expression,

$$(\overline{A} + \overline{B})(\overline{C} + \overline{D})$$

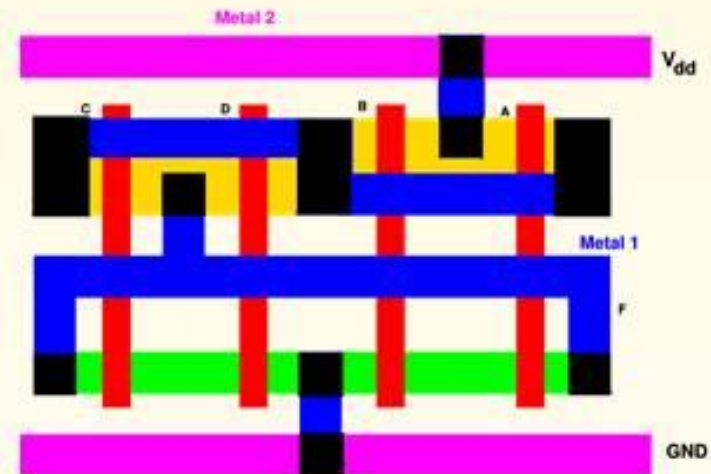
- 5 Combine P and N circuits



Layout of Complex Gate



AND-OR-INVERT (AOI) gate



Note: Arbitrary shapes are not allowed in some nanoscale design rules

Example of Compound Gate

$$F = \overline{(A + B + C) D}$$

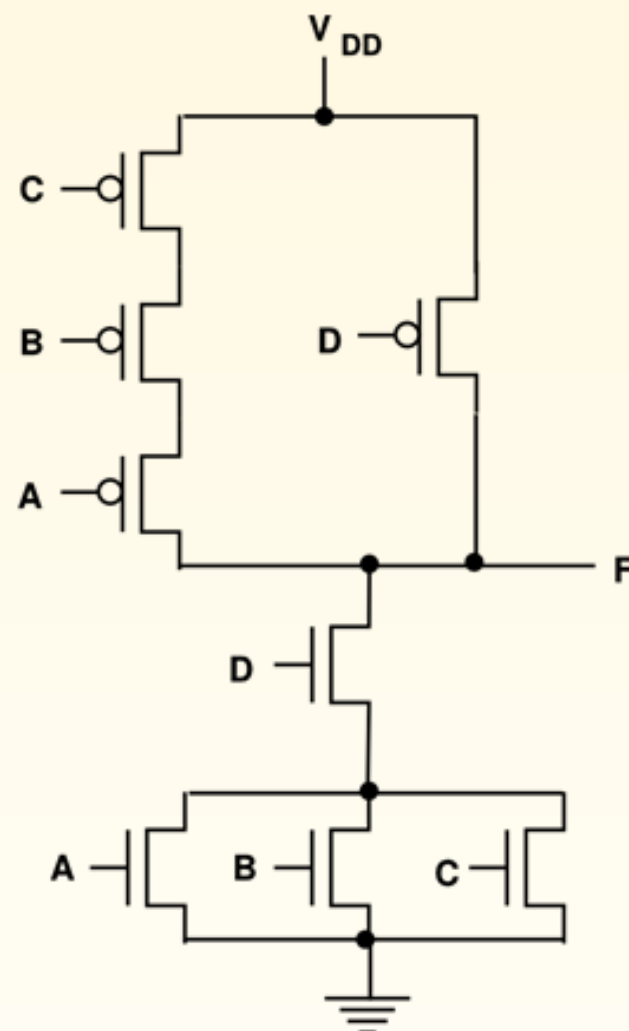
Note:

N- and P- graphs are duals of each other

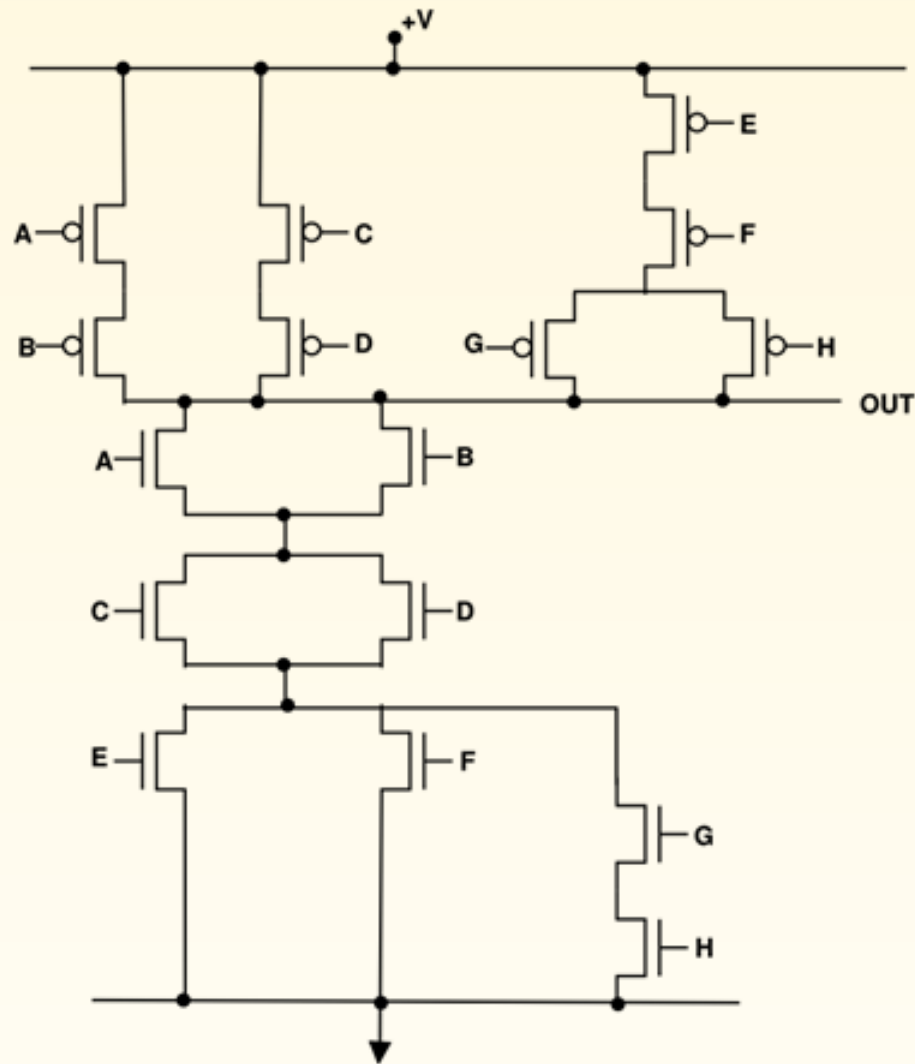
In this case, the function is the complement of the switching function between F and GND

Question: Does it make any difference to the function if the transistor with input D is connected between the parallel A, B, C, transistors and GND?

What about the electrical behavior?

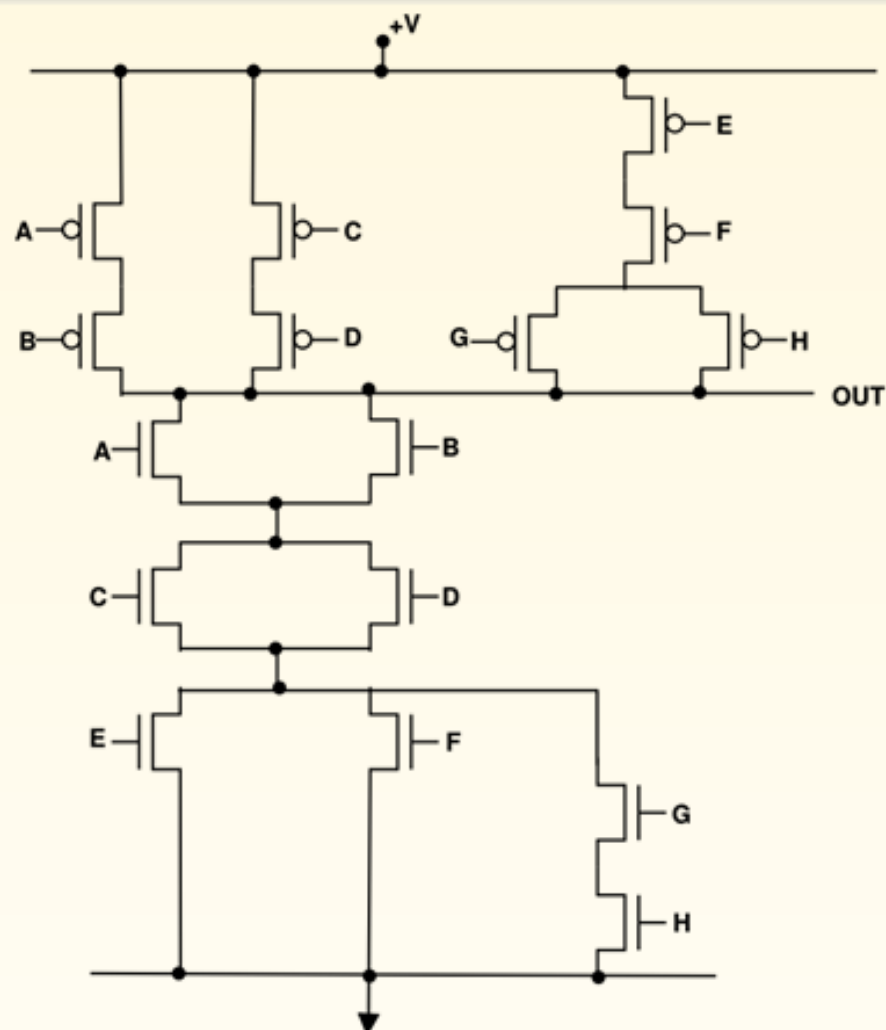


Example of More Complex Gate



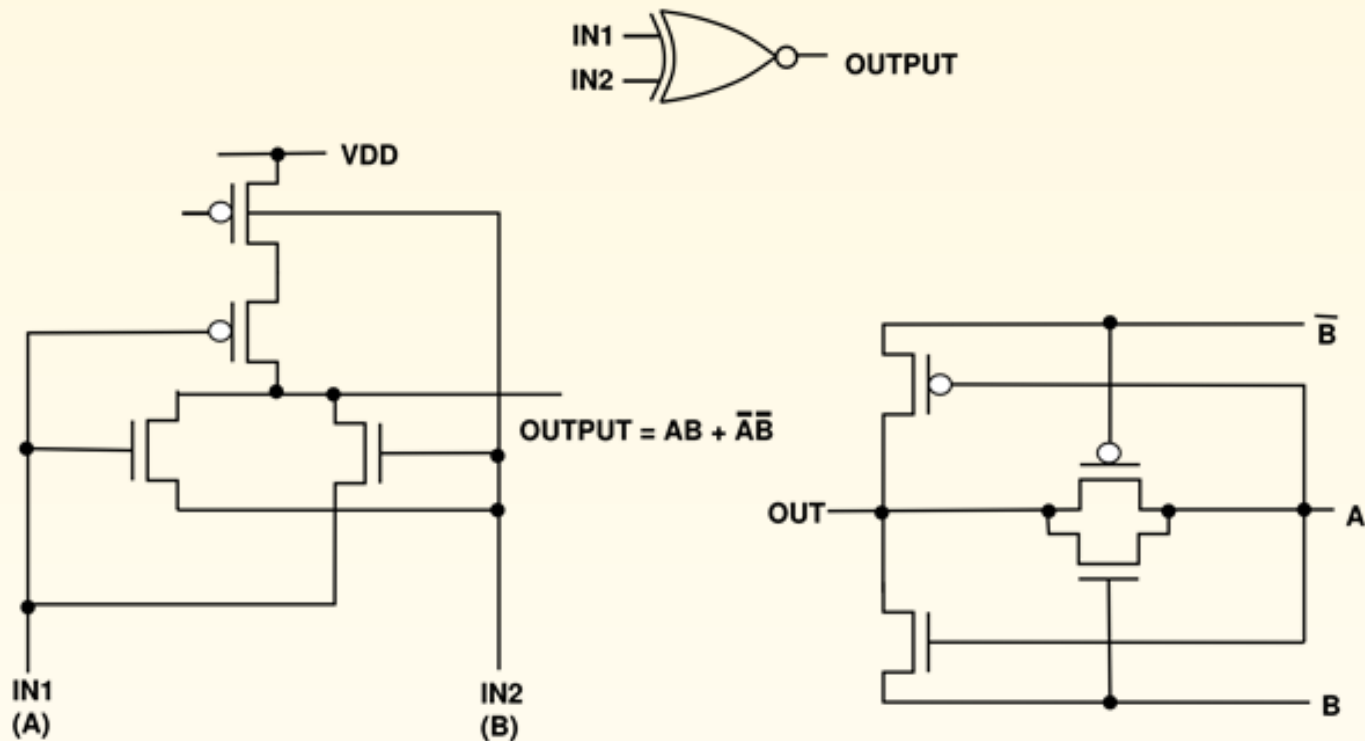
$$OUT = (A + B) (C + D) (E + F + (G H))$$

Example of More Complex Gate



$$OUT = \overline{(A + B) (C + D) (E + F + (G H))}$$

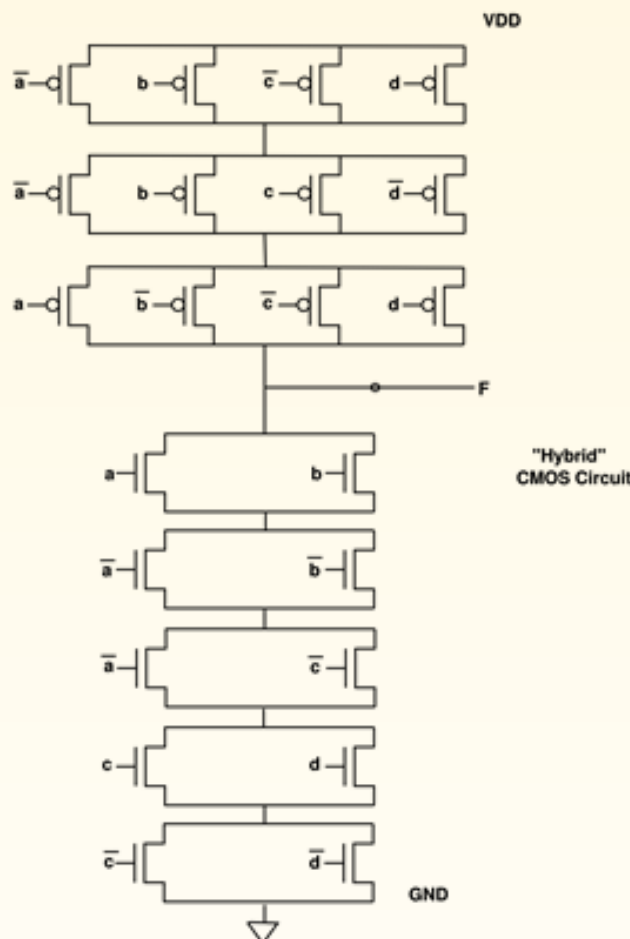
Exclusive-NOR Gate in CMOS



Note: designs such as these should be checked very carefully for correct behavior using circuit simulation

Duality is Not Necessary for a CMOS Structure

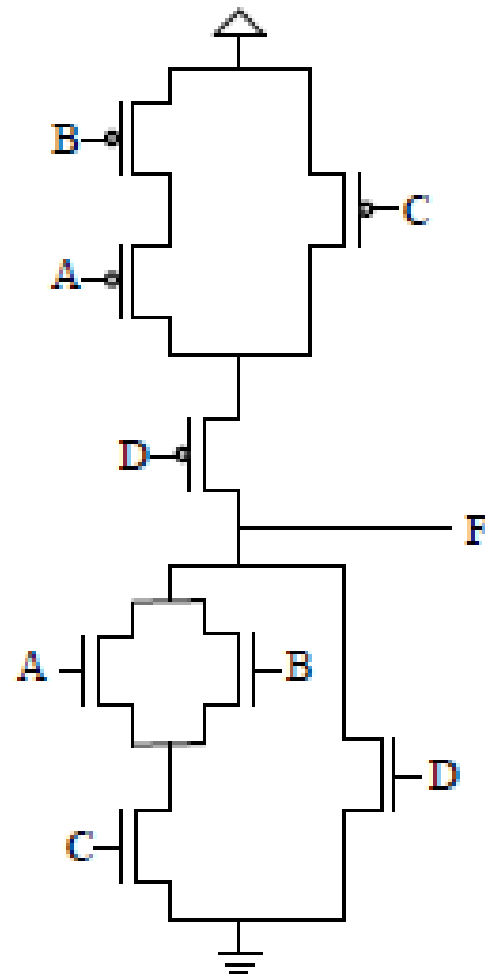
Functions realized by N and P networks must be **complementary**, and one of them must conduct for every input combination



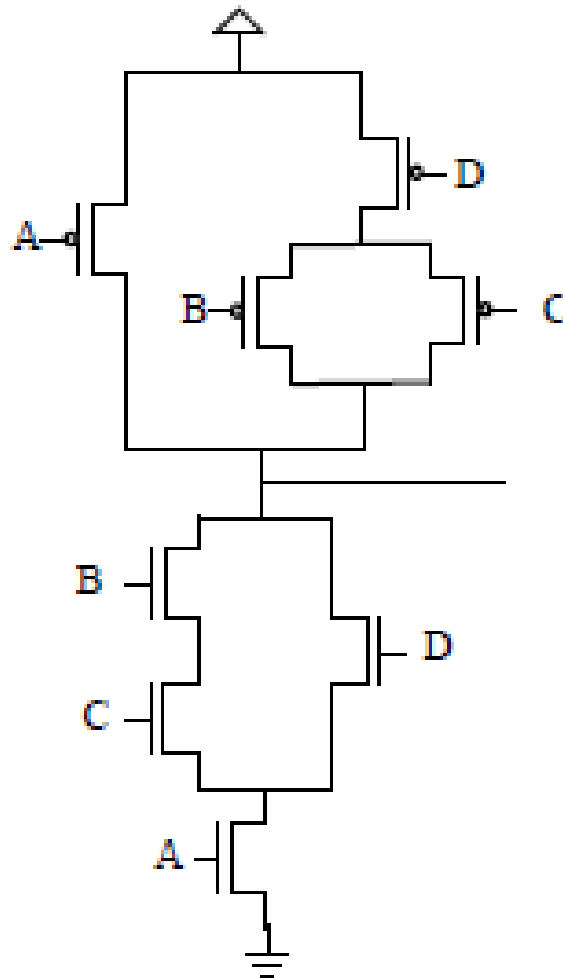
$$F = ab + \bar{a}b + a\bar{c} + cd + c\bar{d}$$

The N and P networks are **NOT duals**, but the **switching functions they implement are complementary**

Please draw the minimum CMOS transistor network that implements the functionality of Boolean equation $F = ((A+B)C + D)'$. You can assume both the original and complemented versions of each literal are available as gate inputs.

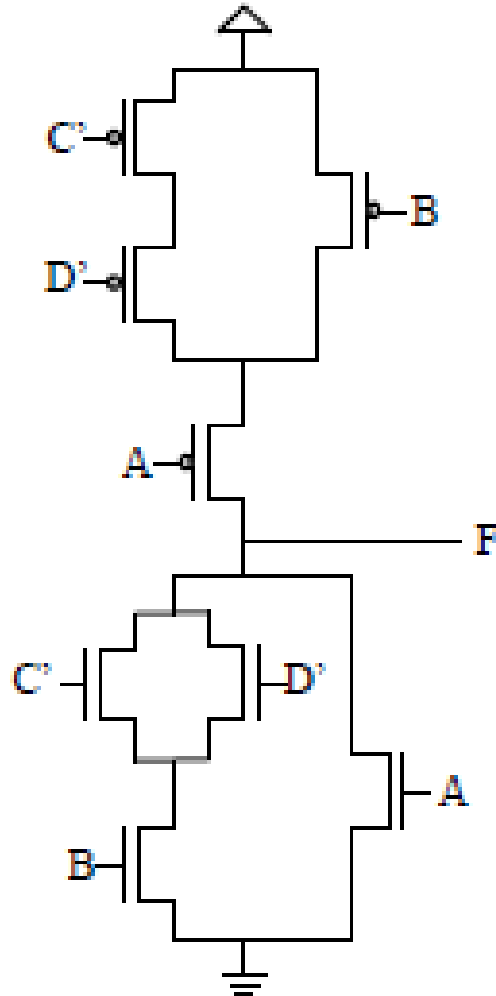


Please draw the minimum CMOS transistor network that implements the functionality of Boolean equation $F = (A(BC + D))'$. You can assume both the original and complemented versions of each literal are available as gate inputs.



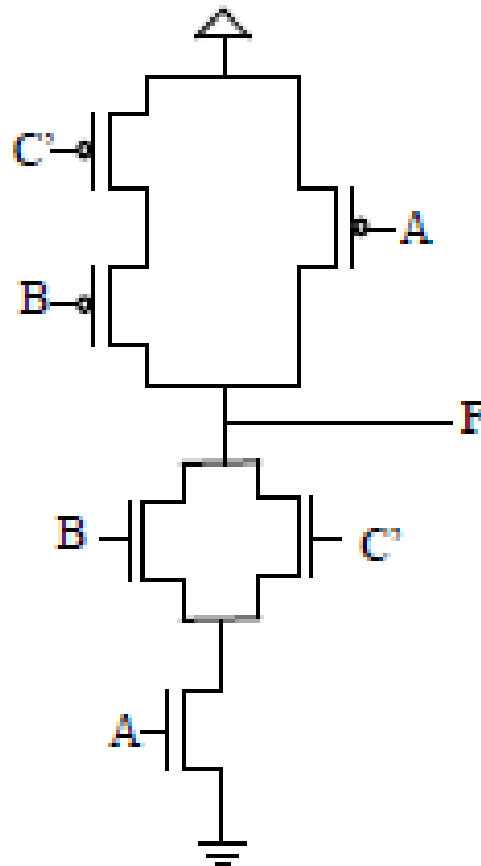
Please draw the minimum CMOS transistor network that implements the functionality of Boolean equation $F = (A + (B' + CD)')'$. You can assume both the original and complemented versions of each literal are available as gate inputs.

$$F = (A + (B' + CD)')' = (A + B(CD)')' = (A + B(C' + D'))'$$



Please draw the minimum CMOS transistor network that implements the functionality of Boolean equation $F = (A' + B'C)$. You can assume both the original and complemented versions of each literal are available as gate inputs.

$$F = (A' + B'C) = ((A' + B'C)')' = (A (B'C)')' = (A (B + C'))'$$



$$1. F = [((CD) + B) A]'$$

$$2. F = (AB)' \text{ since } F = [AB(A+B)]' \text{ on simplification results in } F = (AB)'$$

$$3. F = ((C'+D')B)+A$$

$$F = (A+D+C)(B+E)$$

