VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

School of Computer Science and Engineering

Winter Semester 2023-2024 Continuous Assessment Test – II

SLOT: F2

Programme Name & Branch: B.Tech / BBS

Course Name & code: CBS1004 & Computer Architecture and Organization

Class Number (s): VL2023240503603, 3602

Faculty Name (s): PROF. DILIPKUMAR S , PROF. ANURADHA G

Exam Duration: 90 Min. **Maximum Marks: 50**

Q.No.	Question	Max Marks
1.	What is the control sequence for execution of the instruction MUL R3, R1, R2 (R3 ← R1*R2) including the instruction fetch phase using single bus architecture. Draw the block diagram for necessary operation.	10
2.	A set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16, 384 blocks and each block contains 256 eight bit words. How many bits are required for addressing the main memory? How many bits are needed to represent the TAG, SET and WORD fields? Draw the diagram that represent the hit and miss?	10
3.	A computer employs RAM chips of 128 x 8 and ROM chips of 512 x 8. The computer system needs 256 bytes of RAM, 1024 x 16 of ROM, and two interface units with 256 registers each. A memory mapped I/O configuration is used. a) Compute total number of decoders needed for the above Memory System Design. b) Give the memory-address map for each of the memory chips.	10
4.	A computer has a 1 MB memory with 64 bit word sizes. Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. The computer uses word level addressing. What is the address format? If we change the cache to a 4- way set associative cache, what is the new address format? Draw the diagram that represent the hit and miss.	10
5.	Why does DMA have priority over the CPU when both request a memory transfer? With a suitable diagram Justify.	10