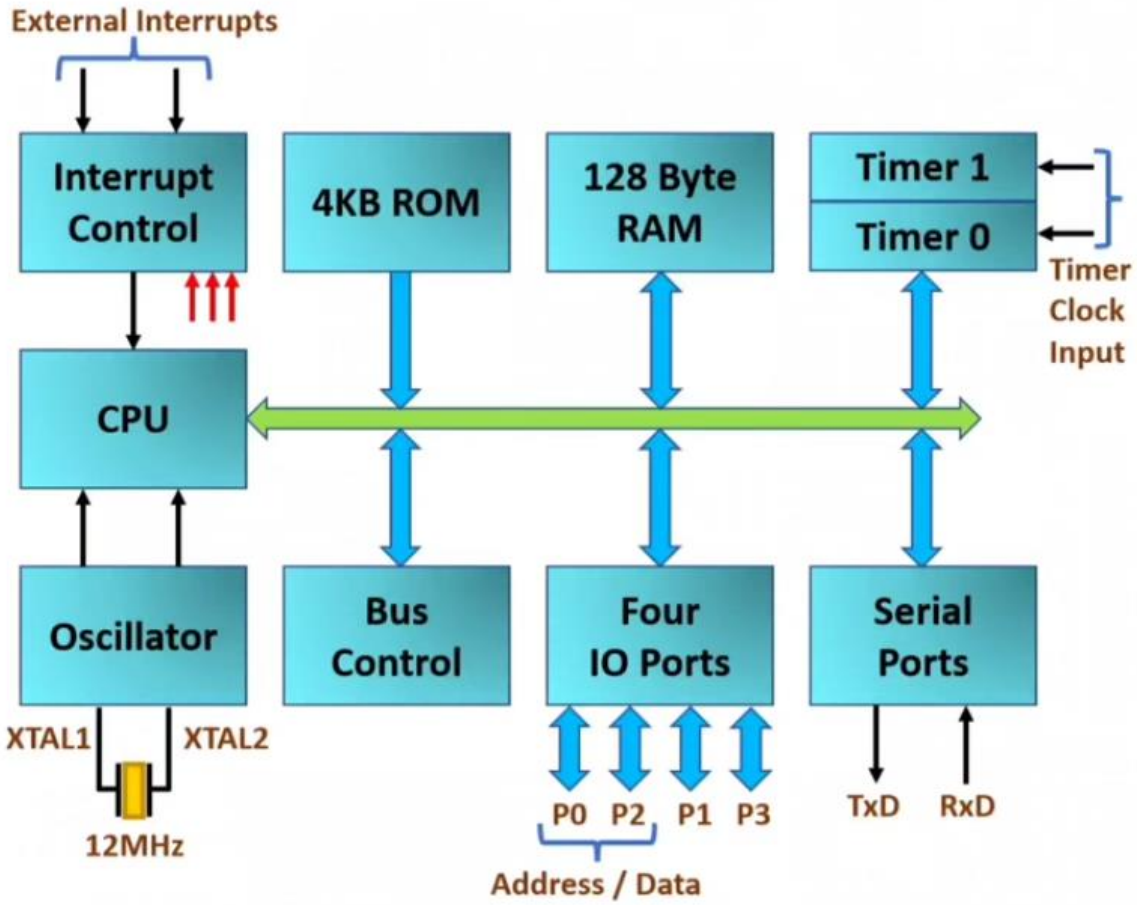
ALU, A, B, PC, DPTR, SP & PSW of 8051



- ALU – Arithmetic & Logic Unit
  - It performs 8 bits of arithmetic & Logic operations.
  - It can also perform one bit operations.
  - Example:

```
ADD A,R1        ;A←A+R1
CPL P0.3        ;Compliment P0.3 pin
```

- Accumulator A
  - Accumulator is 8 bits register.
  - Most of Arithmetic and Logical operations are performed with respect to accumulator.
  - Example:

```
ADD A,R0        ;A←A+R0
ANL A,R1        ;A←A AND R1
```

- Register B
  - It is 8 bits register.
  - It is dedicated for Multiplication and Division.
  - Example:

```
MUL AB          ;BA←A X B
DIV AB          ;A/B, stores quotient in
                A & remainder in B
```

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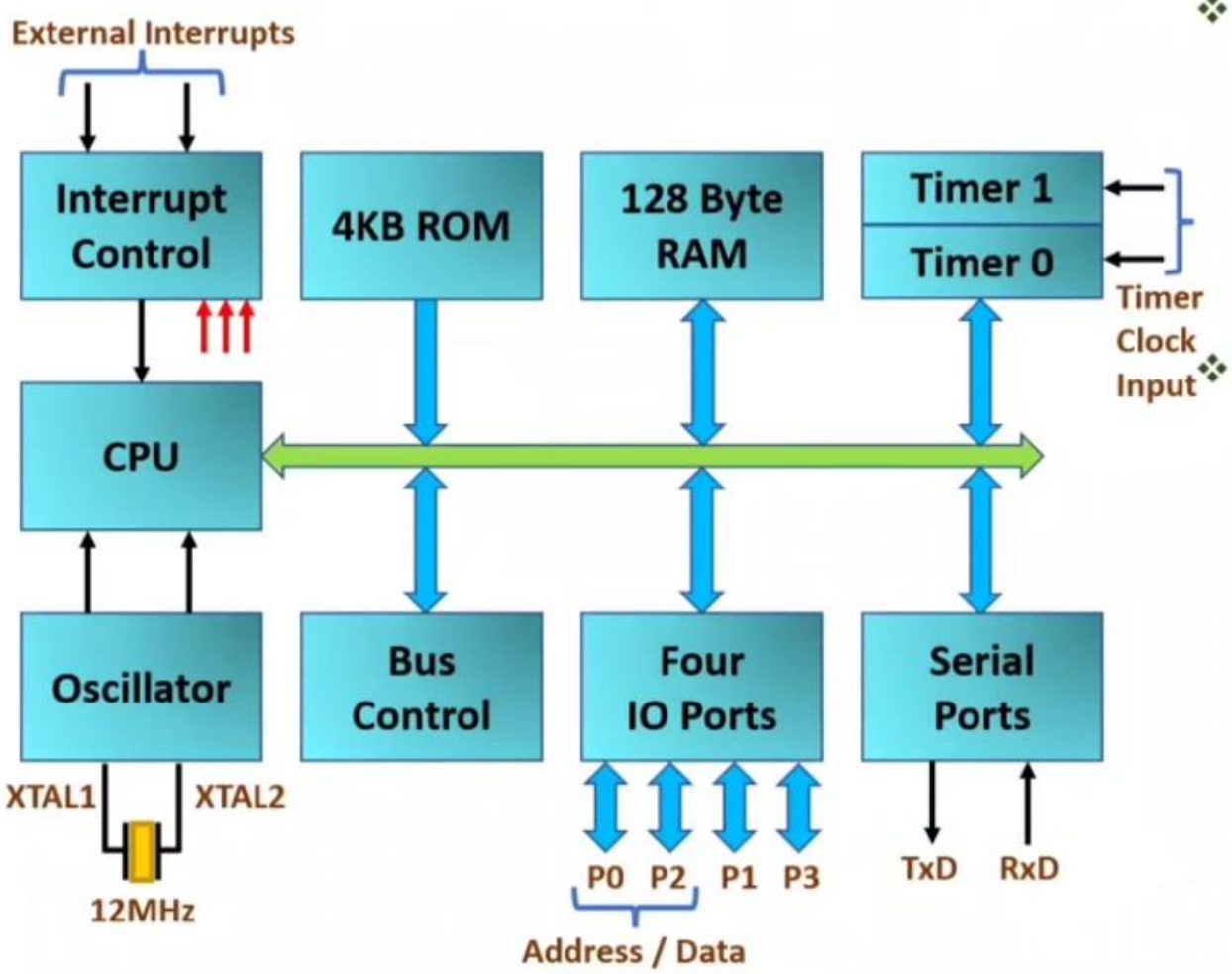
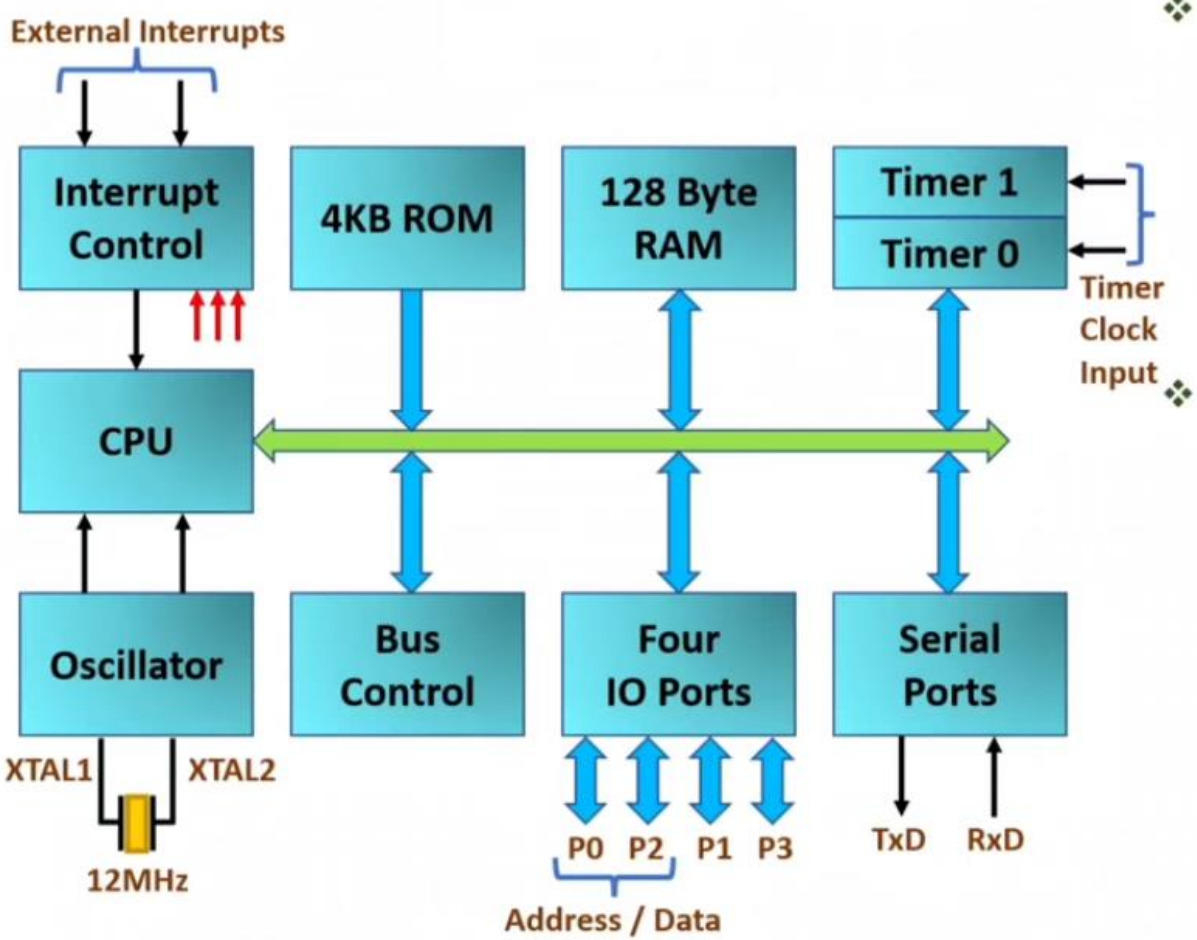


- PC – Program Counter
  - It is 16 bits register.
  - It holds address of next instruction in program memory of ROM.
  - PC gets incremented automatically as soon as any instruction is fetched.
  - In case of branch, new address is loaded in PC.
- DPTR – Data Pointer
  - It is 16 bits register.
  - It holds address of Data in memory of RAM.
  - DPTR is further divided into two registers of 8bits {DPH – Higher Byte & DPL – Lower Byte}.
  - It is used by programmer to transfer data from external RAM.
  - It can also be used as pointer for look up table in ROM, using indexed Addressing Mode.
  - Example:

```
MOVX A,@DPTR     ;A will get data from
                  RAM pointed by DPTR
MOVC A,@A+DPTR;A will get data from
                  ROM pointed by DPTR+A
```

ALU, A, B, PC, DPTR, SP & PSW of 8051



- SP – Stack Pointer
  - It is 8 bits register.
  - It holds address of top of stack.
  - The stack is present in internal RAM.
  - Internal RAM Address is from 00H to 7FH.
  - It is used for PUSH and POP Instructions.
  - On RESET, SP of 8051 indicates 07H address of internal RAM.
- PSW – Program Status Word
  - It is 8 bits register.
  - It is also called the "Flag Register".
  - It gives status after every instruction execution in program.
  - The flags can also be changed by programmer.
  - PSW is bit addressable register.
  - Example:

```
SETB PSW.2      ;PSW.2 = 1
CLR PSW.2       ;PSW.2 = 0
```

PSW / Flag Register in 8051 μC

- P – Parity Flag
  - P = 1, Odd Parity {Odd Number of 1's in result}
  - P = 0, Even Parity {Even Number of 1's in result}
- OVR – Overflow Flag
  - OVR = 1, Signed overflow
  - OVR = 0, No Signed overflow
  - It happens when result goes beyond 127 to -128.
  - After overflow, sign of result {MSB} becomes wrong.
- RS – Register Bank Select
  - RS = 00, Register Bank 0, {Default}
  - RS = 01, Register Bank 1
  - RS = 10, Register Bank 2
  - RS = 11, Register Bank 3
  - By CLR and SETB instructions we can select register bank.
  - Example

```
CLR PSW.4
SETB PSW.3 ;Here RS = 01 means bank 1 is selected
```

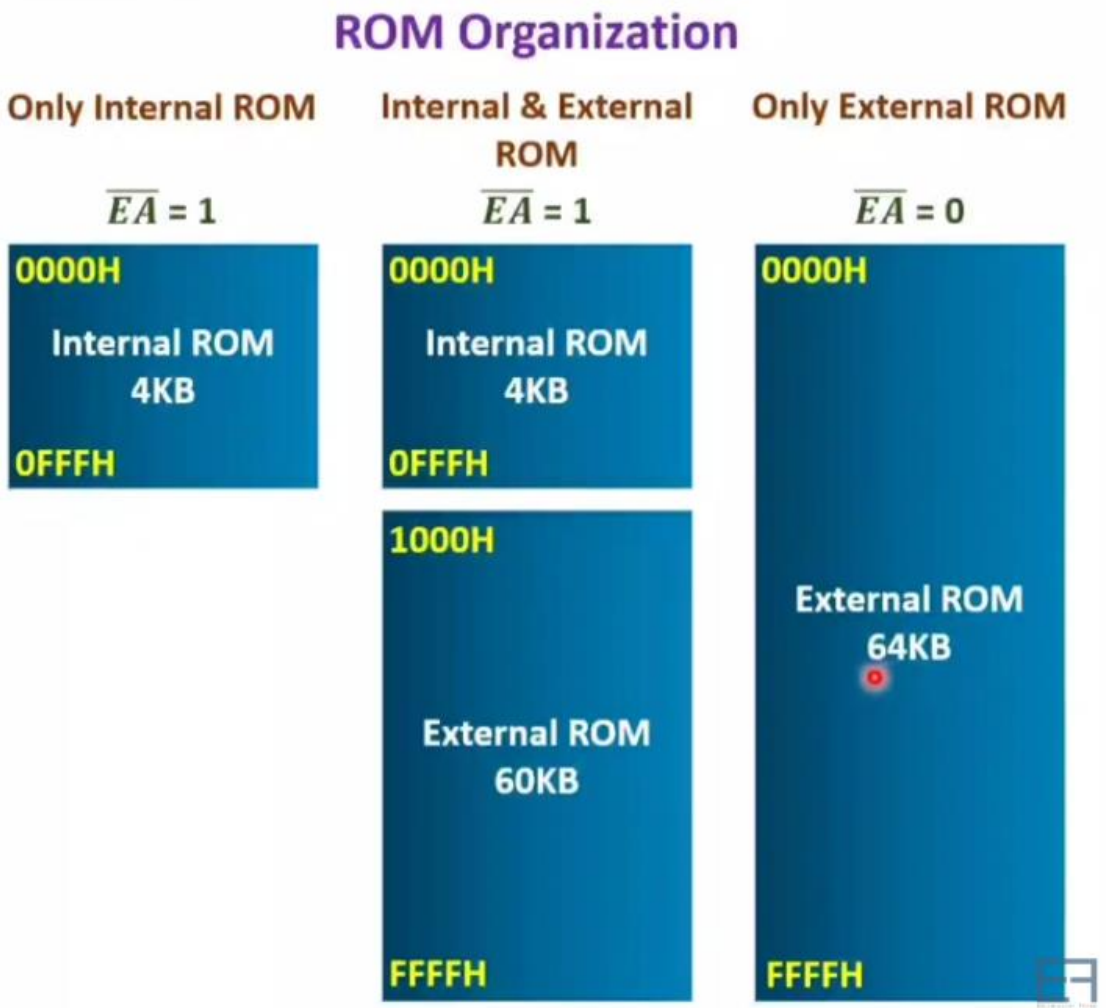
Example:
ADD A,R1

```
          11   1 1
A = CCH   1100 1100
R1 = E6H  1110 0110
-------------------
A = B2H   1011 0010
```

- F0 – User Defined Flag
  - Set by user using SETB PSW.5
  - Clear by user using CLR PSW.5
- AC – Axillary Carry Flag
  - AC = 1, Nibble to Nibble Carry
  - AC = 0, No Nibble to Nibble Carry
- CY – Carry Flag
  - CY = 1, Result has Carry.
  - CY = 0, Result has no Carry.

ROM Organization in 8051 μC

- 8051 Microcontroller Memory
  - 8051 can have four different memories:
    - Internal ROM {4KB}
    - Internal RAM {128 byte}
    - External ROM {Max 64KB}
    - External RAM {Max 64KB}
- Architecture of 8051 Microcontroller
  - 8051 follows Harvard Architecture.
  - So, with 8051 Program memory is ROM and Data memory is RAM.
- Applications of 8051 Microcontroller
  - Microcontroller is used in many embedded system applications. {Remote control, Microwave Oven, Watching Machine etc.}
  - Once controller is embedded in application, program of controller should be fixed and it should be stored in ROM.
  - Data may change in application like time, temperature and it will be stored in RAM.
  - Fixed data will be stored in ROM as look up table. {ASCII, SSD etc.}



Internal RAM Structure in 8051 μC

- 8051 Microcontroller Register Bank in RAM
  - 8051 has four register banks. Each register bank has Eight registers R0-R7.
  - Selection of register bank can be done by two bits of PSW register, by PSW.3 and PSW.4 we can select any register bank.

```
CLR PSW.4
SETB PSW.3        ;Here RS = 01 means bank 1 is selected
```

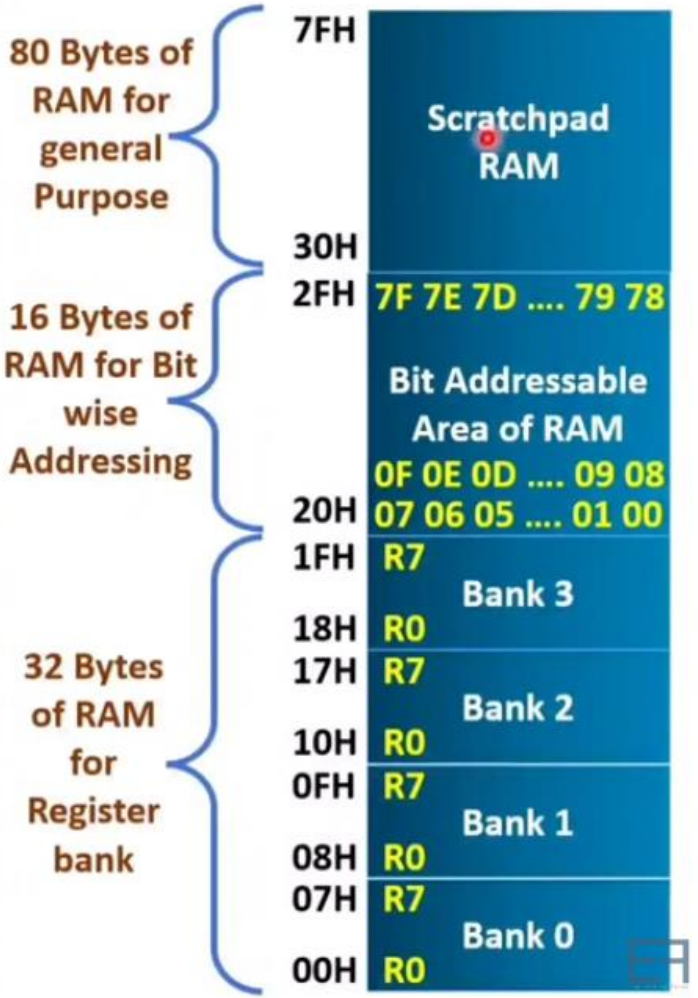
  - RAM address 00H to 1FH holds four register banks.

```
MOV A,R0          ;Copy R0 into A
MOV A,08H         ;Copy R0 of register bank 1 into A
```

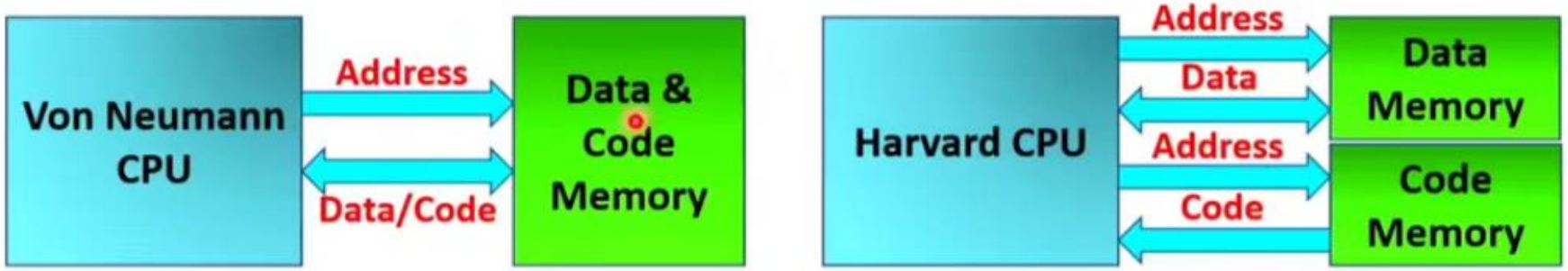
- 8051 Microcontroller Bit Addressable Area in RAM
  - 16 Byte of RAM from 20H to 2FH holds bit addressable area in internal RAM of 8051 microcontroller.
  - 16 x 8 = 128 Addressable bits in these area.
  - These bits are addressed as per 00H to 7FH, in total 128 bits.
  - These locations can have bit as well byte wise operations.

```
SETB 7FH          ;Set MSB of 2FH RAM location
CLR 08H           ;Clear LSB of 21H RAM location
MOV 20H, #FFH     ;Set all bits 20H RAM locations
```

- 8051 Microcontroller General Purpose Area in RAM {Scratchpad RAM}
  - 80 Byte of RAM from 30H to 7FH holds general purpose area in internal RAM of 8051 microcontroller.
  - It can be used for general purpose operations.



Von Neumann Vs Harvard



Parameters	Von Neumann	Harvard
Memory	❖ Data and Program {Code} are stored in same memory	❖ Data and Program {Code} are stored in different memory
Memory Type	❖ It has only RAM for Data & Code	❖ It has RAM for Data and ROM for Code
Buses	❖ Common bus for Address & Data/Code	❖ Separate Bus Address & Data/Code
Program Execution	❖ Code is executed serially and takes more cycles	❖ Code is executed in parallel with data so it takes less cycles.
Data/Code Transfer	❖ Data or Code in one cycle	❖ Data and Code in One cycle
Control Signals	❖ Less	❖ More
Space	❖ It needs less Space	❖ It needs more space