REG.NO.: 24BEI0074

VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SLOT: A2 + TA2

SCHOOL OF ELECTRICAL ENGINEERING
WINTER SEMESTER 2025-2026
CONTINUOUS ASSESSMENT TEST - I

Programme Name & Branch	**: B.Tech. Electrical and Computer Science Engineering**
Course Code and Course Name	**: BECS201L - Semiconductor Devices and Circuits**
Faculty Name(s)	**: Dr. Arunkumar G**
Class Number(s)	**: VL2025260506454**
Date of Examination	**: 27/01/2026, 2.00 to 3.30 PM**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- Rough work should not be done on question paper. It will be treated as malpractice.
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes Statements:

CO. 1: Comprehend the basics of semiconductor materials

CO. 2: Understand the behavior of semiconductor devices and their applications

Q. No	Question	M	CO	BL
1.	Define extrinsic semiconductors. Explain n-type and p-type semiconductors, including the role of donor and acceptor impurities. Also, sketch the necessary diagrams.	10	1	2
2.	Explain the p–n junction diode with neat circuit diagrams for forward and reverse bias. Describe its operation, draw and explain the V–I characteristics, and define static resistance, dynamic resistance, and AC resistance of a diode with a suitable numerical example.	10	2	2
3.	a) An input sinusoidal voltage of 12 V_{p-p} at 50 Hz is applied to a parallel (shunt) diode clipper circuit. The circuit must be designed such that the positive half-cycle of the output is clipped at +4.2 V. Design the clipper (show circuit with component values/levels) and sketch the input and output waveforms, clearly marking the clipping level. Key design data to use (assume): Silicon diode forward drop $V_D \approx 0.7$ V	5	2	3
	b) An input sinusoidal voltage of 12 V_{p-p} at 50 Hz is applied to a positive clamper circuit. Design the clamper such that the positive half-cycle peak of the output is clamped (limited) at +9.5 V. Draw the neat circuit diagram with component values and sketch the input and output waveforms showing the clamping level. Key design data to use (assume): Silicon diode forward drop $V_D \approx 0.7$ V	5		
4.	a) An input sinusoidal voltage of 18 V_{p-p} at 50 Hz is applied to a half-wave rectifier using a silicon diode ($V_D = 0.7$ V) and a load resistor R_L. Determine the average (DC) output voltage V_{avg}, RMS output voltage V_{rms}, and the peak inverse voltage (PIV) of the diode. Write the required design formulae, considering the diode cut-in voltage and sketch the input and output waveforms.	5	2	3
	b) In a BJT CE fixed-bias circuit, $V_{CC} = 12$ V, $V_C = 6$ V, $I_B = 40\,\mu$A, $\beta = 80$, and $V_{BE} = 0.7$ V. Determine R_B, R_C, and I_C.	5		

REG.NO.:

VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SLOT: A2 + TA2

SCHOOL OF ELECTRICAL ENGINEERING
WINTER SEMESTER 2025-2026
CONTINUOUS ASSESSMENT TEST - I

5.	In a BJT CE voltage-divider bias (VDB) circuit, $V_{CC} = 22\,\text{V}$, $R_1 = 39\,k\Omega$, $R_2 = 3.9\,k\Omega$, $R_C = 10\,k\Omega$, $R_E = 1.5\,k\Omega$, and $\beta = 100$. Apply the DC load-line method to sketch the DC load line on the I_C–V_{CE} characteristics, clearly marking the cutoff and saturation points, and indicate the expected operating region / Q-point location on the load line.	10	2	3

****