Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2024-2025

SLOT:C2+TC2

Programme Name & Branch	**: B.Tech CSE**
Course Code and Course Name	**: Computer Architecture and Organization- BCSE205L**
Faculty Name(s)	**: Common to all**
Class Number(s)	**: Common to all**
Date of Examination	**: 18-Mar-2025**
Exam Duration	**: 90 minutes** **Maximum Marks: 50**

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes
  1. Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating point arithmetic operations.
  2. Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.
  3. Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.
  4. Assess the performance of IO and external storage systems. Classify parallel machine models. Analyze the pipeline hazards and solutions.

<table>
<tr><th>Q. No</th><th>Question</th><th>M</th><th>CO</th><th>BL</th></tr>
<tr><td>1.</td><td>Write the assembly code for the given arithmetic statement W=(X+Y)/Z using 0,1,2 and 3 address instructions. Compute memory traffic, memory required to store and encode instructions for 0,1,2 and 3 address machines. Assuming the following fields: addresses - 32 bits, data values -32 bits, opcode - 8 bits and word length - 4 bytes.</td><td>10</td><td>1</td><td>3</td></tr>
<tr><td>2.</td><td>Consider a processor with three instruction classes X, Y and Z, with the corresponding CPI values being 3, 2 and 1 respectively. The processor runs at a clock rate of 2 GHz. For a given program, two compilers produce the following executed instruction counts. Compare the performance of both compilers by computing MIPS and execution time.
<table>
<tr><td></td><td colspan="3">Instruction Count (in millions)</td></tr>
<tr><td></td><td>IC_x</td><td>IC_y</td><td>IC_z</td></tr>
<tr><td>Compiler 1</td><td>4</td><td>5</td><td>6</td></tr>
<tr><td>Compiler 2</td><td>3</td><td>7</td><td>11</td></tr>
</table></td><td>6</td><td>1</td><td>3</td></tr>
<tr><td></td><td>An instruction is stored at location 1000 with its address field at location 1001: the address field has a value of 4000. Address Location 4000 contains 1500. A processor register R1 contains the number 1000 and Index register XR contains the number 200. Evaluate the effective address and content of the accumulator in</td><td>4</td><td></td><td></td></tr>
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REG.NO.:

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	each of the following addressing modes: Direct, Indirect, Relative, Indexed, Register Indirect Addressing Mode.		2	3
3.	A computer employs RAM chips of 1KB and ROM chips of 512 x 8. The computer system needs 1GB of RAM, 4M x 16 of ROM, and two interface units with 256 registers each. A memory mapped I/O configuration is used. The two higher-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers. a. Compute the total number of decoders needed for the above system. b. Design a memory-address map table for the above system. c. Show the chip layout for the above design.	10		
4.	Consider a computer with the following characteristics: total of 1Mbyte of main memory; word size of 1 byte; block size of 16 bytes; and cache size of 64 Kbytes. a. For the main memory addresses of F0010, 01234, and CABBE, give the corresponding tag, cache line address, and word offsets for a direct-mapped cache. b. Give any two main memory addresses with different tags that map to the same cache slot for a direct-mapped cache. c. For the main memory addresses of F0010 and CABBE, give the corresponding tag and offset values for a fully associative cache. d. For the main memory addresses of F0010 and CABBE, give the corresponding tag, cache set, and offset values for a two-way and four-way set-associative cache.	10	2	3
5.	Explain how I/O Controller manages communication between the CPU and peripheral devices in detail with neat diagrams.	4	3	2
	During testing, engineers notice that sometimes the robotic arm does not execute a movement command correctly, especially when the CPU is heavily loaded. Further investigation reveals that some commands are lost, and data transmission errors occur when high-speed operations are performed. • How can implementing a handshaking mechanism between the CPU and the robotic arm improve communication reliability? • How can introducing a buffering technique in the I/O interface help mitigate command loss and improve system performance? • For real-time operations, which approach is more suitable and why?	6		

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