VIT
Vellore Institute of Technology

School of Computer Science Engineering

Winter Semester 2023-2024

Continuous Assessment Test – I

Program Name & Branch: BTECH CSE (BCB, BCE, BCI, BCT, BDS, BKT)

Course Name & code: BECE204L Microprocessors and Microcontrollers

Slot: F1+TF1

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Answer all the questions

S. No	Question	Marks
1.A	Draw the internal architecture of 8051 with a neat sketch	5
1.B	Identify if the following 8051 instruction have any error, if so give the correct instructions (i) DIV A,B (ii) CPL A (iii) PUSH R0 (iv) ORL A, #25H (v) MOV R2, R1	5
2	Analyze the following 8051 assembly program and show the stack and stack pointer during the execution of the program. The address of Bank0 = 00 t0 07H, Bank1 = 08 to 0FH, Bank2 = 10 to 17H and Bank3 = 18 to 1FH. Assume the default stack area.	10

Line No	Instruction	Line No	Instruction
1	SETB PSW.3	10	PUSH 11H
2	MOV R6, #25H	11	PUSH 10H
3	MOV R7,#12H	12	PUSH 0FH
4	SETB PSW.4	13	PUSH 0EH
5	CLR PSW.3	14	POP 0DH
6	MOV R1,#0F3H	15	POP 0CH
7	MOV R2,#0DEH	16	POP 0BH
8	MOV R3.#0FFH	17	POP 0AH
9	PUSH 12H	18	END

3	Assume in the 8051 ROM locations 3000H – 3009H have the values 20H, 31H, 42H, 51H, 62H, 70H, 80H, 90H, 0A1H, and 0B2H respectively. Write an assembly program to perform addition of these ten numbers. Store the carry at 70H and Sum at 71H of RAM. Also write the expected data stored at 70H and 71H of RAM.	10
4	Assume a switch is connected at port pin P1.2, monitor the status of the switch. If the status of the switch is HIGH ("1") then transfer data from R1 (Bank 0) to Port P3, else transfer data from R0 (Bank 0) to Port P3.	10
5	Write an 8051 assembly program to generate a 2ms waveform with 50% duty cycle (Square wave generator) on the port pin P1.5. Assume the clock frequency of 8051 is 12 MHz and use the timer T1.	10