VIT
Vellore Institute of Technology

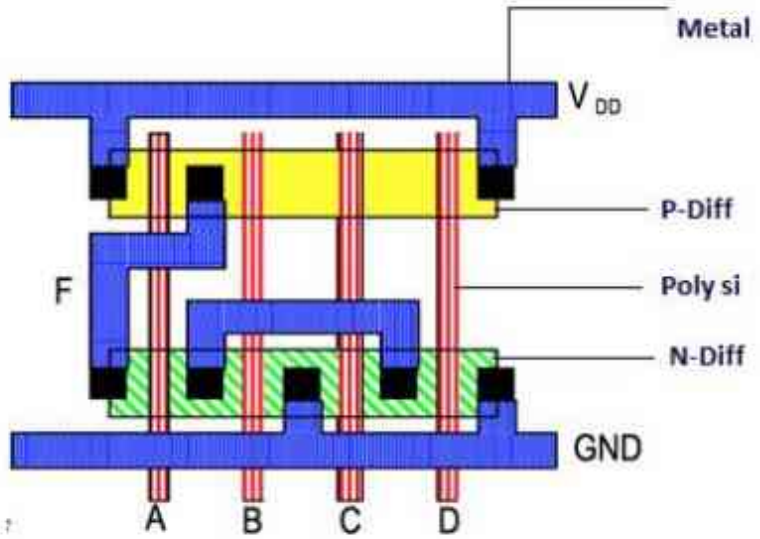
School of Electronics Engineering

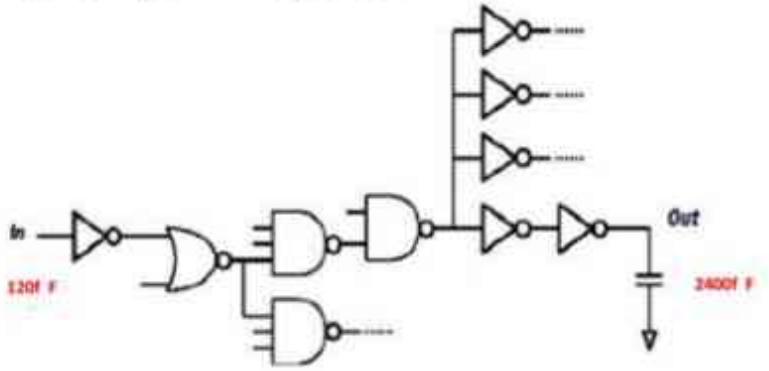
CAT-II

Fall Semester (2022 - 23)

Name of Examination	**CAT-II**		**Fall Semester 2022-23**	
Slot: A1+TA1, A2+TA2			**Class Number (s):** VL2023240100242, 243, 244, 245, 246, 247, 248, 249,250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260	
Course Code:	**BECE303L**	Course Title:	**VLSI System Design**	
Course Mode	**CBL**	Department	MNE	School: SENSE
Duration	**90 Minutes**	Max. Marks	**50 Marks**	

General Instructions (if any): ***Answer all Questions***

S. No	Questions	BL	CO	Marks Allotted
Q1	What is the logic function F implemented by the layout in Figure 1? a) Draw the schematic in terms of MOSFETs b) Determine the truth table and logic function from the truth table c) Estimate the area when the value of λ= 45n for 90nM technology.  Figure 1	BL6	CO 3	10
Q2	Do the sizing of the following circuit Y = $\overline{AB + CD + EF}$ with respect to the reference inverter sizing (PMOS-2 and NMOS-1). Find the worst-case rise time and worst-case fall time for the same.	BL4	CO 4	10

Q3	Calculate the minimum path delay from In to Out for the given network in Figure 2 with output capacitance of 2400fF and input capacitance of 120fF. In order to minimize delay, what should be the size of the gates in the figure from In to Out? Assume the input capacitance of inverter is x (except the first stage inverter), 2 input NAND gate is 2x, 2 input NOR gate is 3x, and 3 input NAND gate is 3x.  Figure 2	**BL5**	**CO 4**	**5+5**
Q4	a) Implement the expression Y = (AB+ C(D + E)) in DCVSL logic and identify the advantages of the logic DCVSL over other logics. b) A system contains a node with a capacitance of 1μF. The supply voltage to the system is 3V, dynamic power dissipation is 10 Watts and the operating frequency is 10MHz. Determine the activity factor.	**BL4**	**CO 4**	**10**
Q5	Implement pass transistor NMOS based 16:1 multiplexer and pass transistor PMOS based 16:1 multiplexer with minimum transistors. The inputs to both the multiplexers are the same (I_0, I_2, I_5, I_9, and I_{12} are 2V and the remaining inputs are 0V). The selection signals to the NMOS-based multiplexers are $S_3S_2S_1S_0$ = 1001, and the selection signals to the PMOS-based multiplexers are $S_3S_2S_1S_0$ = 0111. The threshold voltage of the NMOS and PMOS are 0.5V and 0.8V respectively. Find the output voltages of NMOS based 16:1 multiplexer and PMOS based 16:1 multiplexer.	**BL6**	**CO 4**	**10**