VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

School of Electronics Engineering

CAT I

BECE 102L- Digital Systems Design

Programme & Branch: B. Tech. ECE **Slot: C1+TC1**

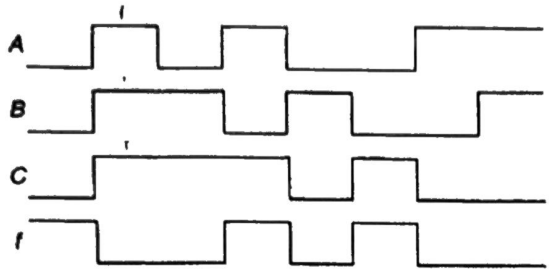
Duration: 90 minutes **Marks: 50**

Class Numbers: VL2022230503275, 3276, 3278

Faculty: Dr Rajesh N, Dr Niroj Kumar Sahu , Dr Sathya P

Answer ALL the Questions

S.No	Question	CO	BTL	Mark
1	(i) Simplify the Boolean function by Boolean algebra F = AB + (AC)'+AB'C (AB+C) (ii) Obtain the canonical POS of the expression F= A+B'C	1	2	5 5
2	Realize the function using (a). AOI logic , (b). NAND only logic (c). NOR only logic F= A'B'+A'C'+B'C'	1	2	10
3	Obtain the (a). minimum SOP and (b). minimum POS of the function F(A,B,C,D)= Σm (0,1,2,5,8,9,10) using 4 variable K – Map	1	3	10
4	Write a gate level modelling program for Full Subtractor.	2	1	10
5	(i) Consider the following inputs to solve the expressions. a = 4'b1011, b=4'b0110, c =4'b 10xx, d=4'b10x1, e= 4'b 10zz y1= (a&e) y2 = (a!=b) y3= (b===c) y4 = (a^b) y5={2{a},{b}}	2	3	5

	(ii) Given the timing diagram of a function. Find the displayed function as sum of minterm in simplified form. Consider A, B, C are the inputs and f is the output.  			5