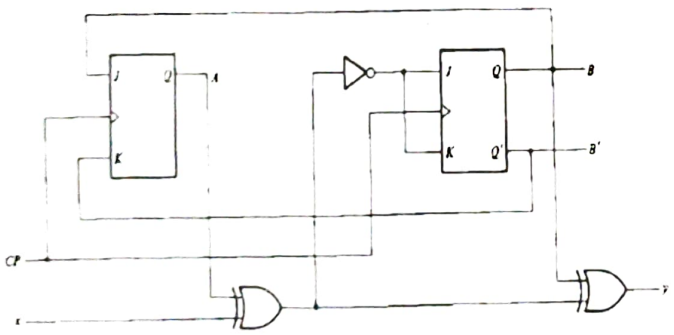
VIT
Vellore Institute of Technology

School of Computer Science Engineering and Information Systems
Winter Semester 2023-24
Continuous Assessment Test – II

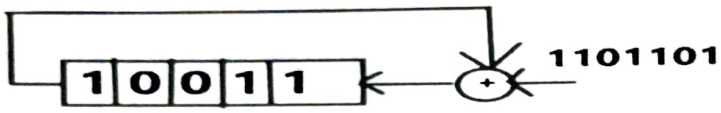
SLOT: D2+TD2

Programme Name & Branch: B.Tech - IT
Course Name & Code: Digital Logic and Microprocessors & BITE202L
Class Number (s): VL2023240503034,VL2023240503037, VL2023240503043
Faculty Name (s): Dr.Malaserene I, Dr.Nithya S, Dr.Karthikeyan D
Exam Duration: 90 Min. **Maximum Marks:** 50

General instruction(s): Answer all the questions

Q. No.	Question	Max Marks
1	Design a sequential circuit with D Flip-flop A and B, two inputs, E and x. If E=1, the circuit remains in the same state regardless of the value of x. When E=0 and x=0, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00 and repeats. When E=0 and x=1, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeats.	10
2	Design a sequential circuit with three flip-flops and one input x. When x = 1, count 0, 1, 3, 5, 7 and repeat. When x = 0, count 7, 5, 1, 3, 0 and repeat. Your answer should include a state diagram and a state table. It should also include Karnaugh-maps and Boolean expressions for each T flip-flop.	10
3	Consider the sequential circuit shown below and analyze it with its input equation, output equations, state table and state diagram. 	10

4	i) Write the physical address for the shown logical address below? 1200:1000 H
	ii)Write the status of flag register after executing the following program:
	MOV AX, 80F0H
	MOV BX, 9010H
	ADD AX, BX
	iii) Write the name of the addressing mode for the following:
	1. MOV AX, 1234H
	2. MOV CL, DL
	3. MOV BX, [1354H]
	4. MOV AX, [SI + 08H]
	5. MOV AX, [BX + SI + 0AH]
		2+3+5

5.	Evaluate the sequence for the following shift registers up to 7 clock pulses and draw the timing diagram for the same. (XOR operation) a)  b)  	5+5

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