



VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

REG.NO.:

SLOT: C1 + TC1

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
FALL SEMESTER 2025-2026

Programme Name & Branch : BCE, BAI, BCB, BCI, BCT, BCT, BDS, BKT
 Course Code and Course Name : BCSE330L and Operating Systems
 Faculty Name(s) : Common to all classes
 Class Number(s) : VL2025260101318, 1332, 1361, 1329, 1364, 1313, 1318, 1336, 1352, 1348, 0589, 1322, 1340, 1320, 1356, 1325, 2374, 1345, 1315
 Date of Examination : 07/10/2025
 Exam Duration : 90 minutes
 Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO - Course Outcome; BL - Blooms Taxonomy Level (1 - Remember, 2 - Understand, 3 - Apply, 4 - Analyse, 5 - Evaluate, 6 - Create)
- Course Outcomes:
 CO2: Design scheduling algorithms to compute and compare various scheduling criteria.
 CO3: Apply and analyze communication between inter process and synchronization techniques.
 CO4: Implement page replacement algorithms, memory management problems and segmentation.

Q. No	Question	Module	Marks	CO	BL																																																																																										
1.	a. A system has two processes and three identical resources. Each process needs a maximum of two resources. Is deadlock possible? Justify the answer? b. Consider the following snapshot of the system: <table><tr><th rowspan="2">Process</th><th colspan="4">Allocation</th><th colspan="4">Max</th><th colspan="4">Available</th></tr><tr><th>A</th><th>B</th><th>C</th><th>D</th><th>A</th><th>B</th><th>C</th><th>D</th><th>A</th><th>B</th><th>C</th><th>D</th></tr><tr><td>P0</td><td>1</td><td>1</td><td>1</td><td>2</td><td>2</td><td>2</td><td>1</td><td>2</td><td>1</td><td>5</td><td>2</td><td>0</td></tr><tr><td>P1</td><td>1</td><td>0</td><td>2</td><td>0</td><td>1</td><td>7</td><td>5</td><td>0</td><td></td><td></td><td></td><td></td></tr><tr><td>P2</td><td>1</td><td>3</td><td>5</td><td>4</td><td>2</td><td>3</td><td>5</td><td>6</td><td></td><td></td><td></td><td></td></tr><tr><td>P3</td><td>0</td><td>6</td><td>3</td><td>2</td><td>0</td><td>6</td><td>5</td><td>2</td><td></td><td></td><td></td><td></td></tr><tr><td>P4</td><td>0</td><td>3</td><td>1</td><td>4</td><td>0</td><td>6</td><td>5</td><td>6</td><td></td><td></td><td></td><td></td></tr></table> Using the Banker's algorithm, determine whether the given resource allocation system is in a safe state, provide the corresponding safe sequence of process execution.	Process	Allocation				Max				Available				A	B	C	D	A	B	C	D	A	B	C	D	P0	1	1	1	2	2	2	1	2	1	5	2	0	P1	1	0	2	0	1	7	5	0					P2	1	3	5	4	2	3	5	6					P3	0	6	3	2	0	6	5	2					P4	0	3	1	4	0	6	5	6					3	3	CO2	BL3
Process	Allocation				Max				Available																																																																																						
	A	B	C	D	A	B	C	D	A	B	C	D																																																																																			
P0	1	1	1	2	2	2	1	2	1	5	2	0																																																																																			
P1	1	0	2	0	1	7	5	0																																																																																							
P2	1	3	5	4	2	3	5	6																																																																																							
P3	0	6	3	2	0	6	5	2																																																																																							
P4	0	3	1	4	0	6	5	6																																																																																							
	7																																																																																														
2.	a. A system contains multiple processes, P_0 to P_{n-1} that need synchronized access to a critical section (CS). Design and explain an algorithm that satisfies the following constraints:	4	6	CO3	BL6																																																																																										



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• Mutual exclusion must be guaranteed (i.e., only one process can enter the critical section at a time). • Unlike the Bakery Algorithm, the solution should not rely on assigning numbers or tickets. • The algorithm should ensure that waiting processes are eventually granted access, preventing starvation and promoting fairness. (If the process is not interested to enter the CS, it will pass the token to the next process in a circular fashion)			
b. <code>#include <stdio.h></code> <code>#include <pthread.h></code> <code>int counter = 0; // Shared variable</code> <code>void* increment(void* arg) {</code> <code> for (int i = 0; i < 10000; i++) {</code> <code> counter++; // Unsafe access – race condition }</code> <code>return NULL;</code> <code>}</code> <code>int main() {</code> <code> pthread_t t1, t2;</code> <code> pthread_create(&t1, NULL, increment, NULL);</code> <code> pthread_create(&t2, NULL, increment, NULL);</code> <code> pthread_join(t1, NULL);</code> <code> pthread_join(t2, NULL);</code> <code> printf("Final counter (without mutex): %d\n",</code> <code>counter);</code> <code>return 0;</code> <code>}</code>		4	



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	Consider the given program where two threads increment a shared counter variable, which leads to a race condition due to concurrent access. Write the pseudo code to demonstrate how to fix this race condition using a critical section with a mutex.				
3.	An airport has a single runway that can be used by either landing or take off operations — but not both at the same time. To avoid crashes, only one plane can use the runway at any given moment. The following conditions must be satisfied: 1. Mutual Exclusion: Only one plane (either landing or taking off) can use the runway at a time. 2. Landing Priority: Planes waiting to land should be given priority over those waiting to take off. 3. No Starvation: Take off planes should eventually get a chance to use the runway once there are no landing planes waiting. Write a pseudocode or algorithm to implement the above scenario using semaphores and mutexes.	4	10	CO3	BL2
4.	a. Consider a system with five memory partitions of sizes (in order): 120 KB, 500 KB, 220 KB, 320 KB, 400 KB. Four processes arrive in sequence: A = 212 KB, B = 95 KB, C = 430 KB, D = 120 KB. Allocate memory for these processes using the following strategies: a. First-Fit b. Best-Fit c. Worst-Fit For each allocation strategy, indicate the partition assigned to each process, display the remaining free space in all partitions after allocation, and evaluate which strategy makes the most efficient use of memory in this scenario. b. Consider a two-level paging hardware with a TLB. Assume that the entire page table and all the pages are in the main memory. It takes 70 milliseconds to access the main memory, and the effective memory access time is measured to be 118 milliseconds. If the TLB hit ratio is 90%, then what is the TLB access time (in milliseconds)?	5	6	CO4	BL5
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5.	a. Consider the following page reference string: 4, 1, 3, 2, 5, 2, 4, 3, 2, 1, 5, 3, 2. How many page faults would occur for the LRU, FIFO and optimal page replacement algorithms assuming 3 and 4 frames?	5	6	CO4	BL3											
	b. Consider the following segment table: <table><tr><th>Segment</th><th>Base</th><th>Length</th></tr><tr><td>0</td><td>1000</td><td>500</td></tr><tr><td>0</td><td>1000</td><td>500</td></tr><tr><td>0</td><td>1000</td><td>500</td></tr><tr><td>1</td><td>2000</td><td>300</td></tr></table> What are the physical addresses for each of the following logical addresses? a. 0, 100 b. 0, 450 c. 0, 600 d. 1, 50		Segment			Base	Length	0	1000	500	0	1000	500	0	1000	500
Segment	Base	Length														
0	1000	500														
0	1000	500														
0	1000	500														
1	2000	300														
