REG. NO.:

SLOT: A2+TA2

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2025-2026

Programme Name & Branch	**: BCE, BAI, BCB, BCI, BCT, BCT, BDS, BKT, BME, BEL, BYB**
Course Code and Course Name	**: BCSE205L & Computer Architecture and Organization**
Class Number(s)	**: Common to All**
Date of Examination	**: 15-03-2026**
Exam Duration	**: 90 minutes**

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Course Outcomes:

CO1: Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machine with different capabilities. Recognize different instruction formats and addressing modes. Validate efficient algorithm for fixed point and floating-point arithmetic operations.

CO2: Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.

CO3 Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.

Q. No	Question	M	CO	BL
1.	A processor executes a program in 6 seconds. The processor operates at a clock rate of 3 GHz. The instruction mix of the program is as follows:	10	CO1	BL3

Instruction Type	CPI	Percentage of Instructions
Arithmetic	1	35%
Memory	3	30%
Branch	4	35%

Assume there are no pipeline stalls other than those reflected in the CPI values.

Calculate the following:

a) The average CPI of the program.
b) The total number of clock cycles executed.
c) The total number of instructions executed.
d) The MIPS rating of the processor during this execution.

Further, assume that after compiler optimization, the branch instruction percentage reduces to 15% (with arithmetic increasing to 50%), and the new average CPI becomes 2.2.

e) Calculate the new execution time.
f) Determine the percentage improvement in performance after optimization.

2	A computer employs RAM chips of 512 x 8 and ROM chips of 128 x 8. The computer system needs 1024 x 16 of RAM, 256 x 16 of ROM, and two interface units with 256 registers each. a. Compute total number of decoders are needed for the above system? b. Design a memory-address map for the above system. c. Show the chip layout for the above design.	10	CO2	BL3

REG. NO.:

SLOT: A2+TA2

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE AND ENGINEERING
CONTINUOUS ASSESSMENT TEST - II
WINTER SEMESTER 2025-2026

3.	a) In cache memory management policies, interpret the following Main Memory block addresses to the cache for FIFO and LRU. Considering a fully associative mapping cache of size 256 bytes with block size 64 bytes, show each step in-detail for hit and miss. 1, 2, 3, 4, 5, 3, 4, 1, 6, 7, 8, 7, 8, 9, 7, 8, 9, 5, 4, 5, 4, 2 Summarize details in the following prescribed format: **Algorithm** | **FIFO** | **LRU** No. of Misses No. of Hits Total no. of Reference Miss Ratio Hit Ratio Compare the results and write your observations.	5	CO2	BL3
	b) A two way set associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The memory address space is 4 GB. Find the number of bits in the TAG and SET fields.	5		
4.	a) Assume in a program variable *j* has 32-bit hex value 0x07654321 in memory starting at address 0x2000. Draw the internal byte storage in big endian and little-endian architectures. Briefly explain one advantage of Little Endian over Big Endian.	5	CO3	BL2
	b) Meera sends a document to the printer and then continues editing another file. The CPU doesn't keep checking the printer's status. Instead, when the printer finishes printing a page, it sends a signal to the CPU, saying, "I'm ready for more data." The CPU then pauses its current work briefly to send the next chunk. Identify the I/O techniques used in the above scenario and justify the answer.	5		
5.	a) Consider a computer system with DMA support. The DMA module transfers one 8-bit character in one CPU cycle from a device to memory through cycle stealing at regular intervals. If the DMA clock frequency is 2 MHz, calculate the data transfer rate of the device in bits per second.	4	CO3	BL3
	b) In a research workstation, the CPU is engaged in executing a real-time simulation that requires continuous responsiveness while simultaneously handling background data transfers from multiple devices. Two DMA requests occur in close succession: one from a satellite sensor module that streams data at a sustained rate of 500 KB/sec, sending packets of 4 KB each into main memory, and another from a solid-state storage unit that transfers a 10 MB dataset into memory. During the sensor transfer, the CPU continues execution but experiences intermittent slowdowns, whereas during the storage transfer, the CPU undergoes longer pauses and is unable to access the bus until large chunks of data are fully moved. From these observations, analyze the CPU behaviour and the characteristics of each transfer to determine the corresponding DMA modes of operation, providing justification in terms of bus control duration, CPU responsiveness, and the nature of the data being transferred.	6		