REG.NO.:

VIT
Vellore Institute of Technology

NAME OF THE SCHOOL
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2024-2025

SLOT: B2+TB2

Programme Name & Branch	**: B.Tech- Information Technology**
Course Code and Course Name	**:BITE202L -Digital Logic and Microprocessors**
Faculty Name(s)	**: Prof. Santhi.K, Prof. Pradeepa.M, Prof. Nithya.S Prof. Krishnamoorthy.N**
Class Number(s)	**: VL2024250502972,VL2024250502974, VL2024250502959, VL2024250502968**
Date of Examination	**: 28-Jan-2025**
Exam Duration	**: 90 minutes**

Maximum Marks: 50

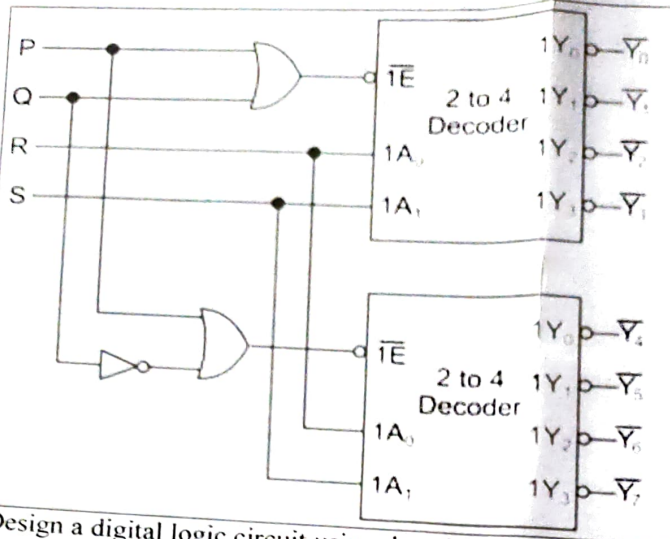
General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)
- Course Outcomes (Type the CO statements covered in this question paper. Use the CO number as per the syllabus copy)

CO 1.Understanding the structure of various number systems and Illustrate simplification of Boolean functions to achieve optimized design of digital logic circuits.

CO 2. Demonstrate the design, and analysis of various combinational logic circuits and Sequential logic circuits using flip flops and logic gates.

Q. No	Question	M	CO	BL
1.	i) a) Find the 10's complement of 3250 b) Convert $(BABA.B)_{16}$ to binary. c) Convert $(35.125)_{10}$ to octal. d) Find the binary number, whose 2's complement will result the original binary number.	4	CO1	BL2
	ii) Implement the following logical expression only by using NAND gates after simplification. F(A, B, C, D) = AD + BC'D'+ ABC + A'BC'D	6		
2.	Simplify the following Boolean functions, using five-variable K-map: F (A, B, C, D,E) = ∑ (0,5,6,8,9,10,11,16,20,24,25,26,27,29,31)	10	CO1	BL3
3.	Design a combinational circuit that converts a four-bit Binary code B3, B2, B1and B0 to a four-bit gray number G3, G2, G1and G0. Implement the circuit with exclusive-OR gates.	10	CO2	BL3
4.	a) Implement Full Subtractor circuit using 1-to-8 De-Mux and a minimal number of basic logic gates	5	CO2	BL3
	b) A 1 to 8 de multiplexer with data input Din, address inputs S0, S1, and S2, (with S0 as the LSB) and $\bar{Y}0$ to $\bar{Y}7$ as the eight de-multiplexed output, is to be designed using two 2 to 4 decoders (with enable input E and address input A0 and A1) as shown in the figure. Din, S0, S1, and S2 are to be connected to P, Q, R, and S but not necessarily in this order. Identify the appropriate respective input connections to P, Q, R, and S terminals and justify your answer.	5		



5.	Design a digital logic circuit using decoders to monitor water quality. Water is not safe ("Logic 0") to drink under the anyone of the following scenarios: a) If the pH sensor cross the appropriate pH range 6.5 and 8.5 b) If the turbidity sensor reading goes below 50 NTU and temperature sensor cross the appropriate range 10°C - 30°C. c) If dissolved oxygen is above 5 mg/L. Otherwise water can be considered as safe ("Logic 1") to drink. pH sensor output will be "Logic 1" if pH is between 6.5 and 8.5. Otherwise "Logic 0". Turbidity sensor output will be "Logic 0" if Turbidity is less than 50 NTU. Otherwise "Logic 1" Dissolved Oxygen sensor output is "Logic 1" if the reading is above 5 mg/L. Otherwise "Logic 0". Temperature sensor output is "Logic 0" if temperature lies in range 10°C - 30°C. Otherwise "Logic 1" Construct the truth table, canonical and standard expression for the above application. Realize the logic circuit using decoder.	10	CO2	BL3

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