Ca/D/TZ

Reg. No:

VIT®
Vellore Institute of Technology

Final Assessment Test – April 2026

Course: **BEVD207L - Computer Architecture**

Class NBR(s): **0889 / 0891** Slot: **D1+TD1**

Time: **Three Hours** Max. Marks: **100**

- **KEEPING MOBILE PHONE/ANY ELECTRONIC GADGETS, EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

COs	CO Statements
CO1	Understand the basic structure of computers, operations, and instructions.
CO2	Understand the arithmetic and logic unit and implementation of fixed-point and floating-point arithmetic units.
CO3	Understand the various memory systems.
CO4	Understand the processor design control unit.
CO5	Understand parallel processing and pipelined execution.
CO6	Comprehend the methods of performance enhancement techniques such as pipelining and their hazards, Scalar and Vector processing architectures, and Multiprocessing techniques like SMP

BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

Answer ALL Questions
(10 X 10 = 100 Marks)

1.	Compare Von-Neumann and Harvard architecture by illustrating its block diagrams, respectively.	CO1	BL1
2.(a)	Represent the given numbers $A = (-0.40)_{10}$, and $B = (1.25)_{10}$ in half precision floating-point format (*fp16*) as A_{fp16} and B_{fp16}. Also, determine $C_{fp16} = A_{fp16} \times B_{fp16}$ using the floating-point multiplication algorithm.	CO2	BL2
	OR		
2.(b)	Explain the Long/Restoring division algorithm with a necessary flow chart. Verify the algorithm using the dividend, $Q = (7)_{10}$ and divisor, $M = (-3)_{10}$.	CO2	BL2
3.	Design a 16-bit memory of total capacity 8192 bits using SRAM chips of size 64 × 1 bit. Give the array configuration of the chips on the memory board, showing all required input and output signals for assigning this memory to the lowest address space. The design should allow for both byte and 16-bit word accesses.	CO3	BL3
4.	Explain the purpose and operation of the Translation Lookaside Buffer scheme with the necessary illustrations.	CO3	BL1

5. List and explain the types of instructions, with respect to operations and the number of addresses. Give at least one example for each. **CO4 BL2**

6. Explain hardwired control logic for a typical ALU. What are the drawbacks of hardwired logic, and how microprogramming used to solve this? **CO4 BL1**

7.(a) Assuming delayed branching, rewrite the below given code to take advantage of the branch delay slot. Show the timing of the below instruction sequence for the 5-stage MIPS pipeline with full forwarding hardware. How many cycles does this loop take to execute? What is the average CPI? **CO5 BL2**

```
I1: LD R1,R2    ;load R1 =Memory( R2)
ADD  R1,R1,1 ; R1= R1+1
SD R1,R2        ;Store memory(R2) =R1
ADD R4,R4,-1  ;R4 =R4+(-1)
BNE R4,R0,I1 ;Branch if R4!= 0
ADD R2,R2,8  ;R2 =R2+8
```

OR

7.(b) Consider a computer that has four categories of instructions. The name and CPI (Cycles Per Instruction) of each category are listed in Table 1. **CO5 BL2**

Table 1:

Category	CPI (Cycle Per Instruction)
Integer	2
Load/Store	4
Branch	3
Floating point	8

A program is running on this computer. This program consists of 40% Integer arithmetic, 25% load/store operations, 30% branch instructions, and 5% floating-point operations.

i) What's the CPI of this program running on this computer?

ii) Now, there are two schemes for improving the performance of this computer. Find which scheme is better for deployment as the scheme informations listed below.

Scheme (A) enhances the performance of FPU, allowing the CPI of floating-point operations to be reduced to 4.

Scheme (B) adds a write buffer to reduce the CPI of the store instruction to 1. The instruction mix of the testing program is the same as a). Also, assume 20% of load/store instructions are store instructions.

8.	(a) What is the speed-up of the 12-stage pipeline over the 5-stage pipeline, considering only data hazards?	CO5	BL1
	(b) Describe what forwarding paths are needed for the rearranged pipeline by stating the source stage, destination stage, and information transferred on each needed new path. Give an instruction sequence showing each data hazard that can be resolved by forwarding data between stages. Draw a timing diagram showing the forwarding between the stages.		
9.	(a) Explain why memory fences are required even in coherent systems.	CO6	BL1
	(b) Differentiate symmetric and distributed shared memory architectures.		
10.	(a) Explain the basic structure and salient features of a Vector Processor.	CO6	BL1
	(b) Compare vector-register architectures with memory-memory vector architectures.		

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