REG.NO.: 24BIT0025

SLOT: G2+TG2

VIT

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF COMPUTER SCIENCE ENGINEERING AND INFORMATION SYSTEMS
CONTINUOUS ASSESSMENT TEST - I
WINTER SEMESTER 2025-2026

Programme Name & Branch	: B.Tech – Information Technology
Course Code and Course Name	: BITE301L & Computer Architecture and Organization
Faculty Name(s)	: Dr.SUMATHY S, Dr.SUMATHI D, Dr. KRISHNAMOORTHY N, & Dr. MEENATCHI S.
Class Number(s)	: VL2025260502752, 755, 757, 760
Date of Examination	: 02.02.2026
Exam Duration	: 90 minutes

Maximum Marks: 50

General instruction(s):

- Answer All Questions
- M - Max mark; CO – Course Outcome; BL – Blooms Taxonomy Level (1 – Remember, 2 – Understand, 3 – Apply, 4 – Analyse, 5 – Evaluate, 6 – Create)

CO 1: Elucidate the arithmetic operations, addressing modes and the performance of Computers

CO2: Design instruction level parallelism using instruction stages. Understand pipelining concepts and identify the hazards to rectify in typical processer pipeline

Q. No	Question	Module	Marks	CO	BL
1.	a) A computer system is designed with a high-speed CPU, main memory, and several I/O devices such as a keyboard, printer, and storage devices. Initially, all components are connected using a single shared bus. During system operation, it is observed that the CPU frequently waits for bus access due to simultaneous I/O requests, leading to reduced system performance. Additionally, the I/O devices operate at speeds much slower than the processor and memory. To overcome these issues, what the system designer should proposes.	1	5	1	BL2
	b) Compare and contrast CISC and RISC architectures by discussing at least five valid points highlighting their advantages and disadvantages.		5		
2.	a) Processor P has a clock speed of 2.5 GHz and a clock cycles per instruction (CPI) of 3 for a given program with 200 million instructions. If improvements in the architecture reduce the CPI to 2.5 without changing the clock speed and no of instructions, i. Calculate the old and new execution time (4) ii. Calculate the reduction in execution time (2) iii. Percentage improvement in performance. (2)	1	10	1	BL4
	b) A program executes on a 1 GHz processor with an average CPI of 2 and completes in 5 ms. Determine the total number of instructions executed by the program. (2)				

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3.	Develop program to evaluate the arithmetic expression. X=A*B+C*D+E-F. 1. Using a general register computer with three address instructions. 2. Using a general register computer with two address instructions. 3. Using an accumulator type computer with one address instructions. 4. Using a stack organized computer with zero-address operation instructions. Where X, A, B, C, D, E and F are memory addresses. In accordance with programming language practice, computing the expression should not change the original value of its operands.	2	10	2	BL3
4.	An instruction is stored in main memory at address location 1000, and its address field is located at memory address 1001. The value stored in the address field is 600. Standard assumption: the instruction is LOAD AC ← operand. At the time of execution, the processor registers contain the following values: • R1 = 900 • XR (Index Register) = 200 • PC = 400 • BR (Base Register) = 700 The contents of selected memory locations are given below a) Determine the effective address (EA) for the instruction under each of the following addressing modes. b) Determine the contents of the Accumulator (AC) for the provided data, assuming the instruction uses the following addressing mode. 1. Immediate addressing mode 2. Direct addressing mode 3. Indirect addressing mode 4. Register addressing mode 5. Register indirect addressing mode 6. Pre increment addressing mode 7. Auto decrement addressing mode 8. Relative addressing mode 9. Base addressing Register mode 10. Indexed addressing mode	2	10	2	BL4

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Memory Address	Value
600	700
601	800
602	900
700	950
800	990
899	980
900	1000
901	1050
1000	1150
1100	1200
1300	1700
1500	1800

5.	a) A processor uses an instruction pipeline with 4 stages. A program consisting of 20 instructions is to be executed on this processor. The clock cycle time of the pipeline is 10 ns. Based on the above scenario, answer the following: i. Calculate the total execution time for executing the program without pipelining (sequential execution).(1) ii. Determine the total execution time for executing the program using pipelining. (1) iii. Compute the speedup achieved due to pipelining.(2) iv. Calculate the efficiency of the pipeline.(2)				
	b) A pipeline is used to improve the speed of execution of a program. Assume an ARM9 processor with a 5-stage instruction pipeline consisting of the following stages: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Consider that 8 instructions (I1 to I8) are to be executed. i. Determine the total number of clock cycles required to execute all instructions without pipelining (sequential execution).(2) ii. Determine the total number of clock cycles required to execute the same instructions using ideal pipelined (parallel) execution.(2)	2	10	2	BL4