VIT

Vellore Institute of Technology

School of Computer Science and Engineering

Fall Semester 2022-2023

Continuous Assessment Test – I

Programme Name & Branch : BTECH CSE **SLOT: D1+TD1**

Course Name & code: Digital Systems Design BECE102L

Class Number (s): VL2022230104419, VL2022230104429, VL2022230104434, VL2022230104441, VL2022230104438, VL2022230104439, VL2022230104441, VL2022230104443, VL2022230104446, VL2022230104572, VL2022230104574

Faculty Name (s): JAYAKRISHNAN P, SHWETA B THOMAS, MANGAIYARKARASI R, DEBASHIS MAJI, SUMIT KUMAR JINDAL, RAJESH G, DEBASHISH DASH, ANJU THOMAS, VIKAS VIJAYVARGIYA, KUMARANARAYANA SWAMY C, DINAH ANN VARUGHESE

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Mention the question number outside the margin clearly. Answer in sequential order with clarity. Draw the diagrams neatly using appropriate pencil and scale.

Q. No.	Questions	Max Marks	CO	BL
1.	Simplify the Boolean expression using theorems and postulates. Draw the logic diagram using logic gates for the simplified Boolean expression a) $Y = A'B + B'C + C + A'B'C'D' + C'D'$ b) $F(a,b,c,d) = \sum m(0,1,3,8,9,13,15)$	5 5	CO 1	BL2

2.	a. Explain with an example how digital gates are implemented using CMOS technology.
	b. Find the syntax errors in the following declarations (note that names for primitive gates are optional):
	module module Exmpl-3(A, B, C, D, F) // Line 1
	inputs A, B, C, Output D, F, // Line 2
	output B // Line 3
	and g1(A, B, D); // Line 4
		5
		5
			CO 2	BL2

	not (D, A, C), // Line 5
	OR (F, B; C); // Line 6
	endmodule // Line 7			

3.	Use K-maps to find the minimum-cost SOP and POS expressions for the function and draw the corresponding logic diagrams of SOP and POS expressions $F(a, b, c, d) = a'c'd' + cd + a'b'd + abc'd$	10	CO 1	BL3
4.	Design a combinational circuit with three inputs and one output. Draw the corresponding truth table and Logic diagrams. (a) The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise. (b) The output is 1 when the binary value of the inputs is an even number.	 5 5	CO 1	BL2
5.	Draw the truth table and logic diagram of the digital circuit specified by the following Verilog description: **module** Circuit_B (F1, F2, F3, A0, A1, B0, B1); **output** F1, F2, F3; **input** A0, A1, B0, B1; **nor** (F1, F2, F3); **or** (F2, w1, w2, w3); **and** (F3, w4, w5); **and** (w1, w6, B1); **or** (w2, w6, w7, B0); **and** (w3, w7, B0, B1); **not** (w6, A1); **not** (w7, A0); **xor** (w4, A1, B1); **xnor** (w5, A0, B0); **endmodule**	10	CO 2	BL3

NOTE*: Please refer below to the BL – Bloom's Taxonomy Levels and mention the respective level in the questions.

Bloom's Taxonomy Levels	Category
BL1	Remembering
BL2	Understanding
BL3	Applying
BL4	Analyzing
BL5	Evaluating
BL6	Creating