J/E/TX

Reg. No: 23BIT0161

VIT
Vellore Institute of Technology

Final Assessment Test – May 2024

Course: **BITE202L - Digital Logic and Microprocessors**
Class NBR(s): **3035 / 3036 / 3040** Slot: **D1+TD1**
Time: **Three Hours** Max. Marks: **100**

- **KEEPING MOBILE PHONE/ELECTRONIC DEVICES EVEN IN 'OFF' POSITION IS TREATED AS EXAM MALPRACTICE**
- **DON'T WRITE ANYTHING ON THE QUESTION PAPER**

Answer any TEN Questions
(10 X 10 = 100 Marks)

1. a) Convert the following decimal number to the indicated bases: **[5]**

   $175.175=(\ )_2=(\ )_8$

   b) Simplify the given Boolean functions in product of sums using K map and draw the circuit using NAND gate only. **[5]**

   $F(A,B,C,D)=\Pi(1,3,5,7,13,15)$

2. Solve the sum of products expression using 5 variable K map and draw the logic circuit.

   $F(A,B,C,D,E)=\sum_m=(0,1,4,5,13,15,20,21,22,23,24,26,28,30,31)$

3. a) Design a combinational circuit that converts a 3-bit Gray code to a 3-bit binary number. Implement the circuit with Exclusive-OR gates. **[5]**

   b) Design a 4 bit adder/subtractor circuit with one selection variable M and two inputs A($A_3A_2A_1A_0$) and B ($B_3B_2B_1B_0$)using MSI circuit. **[5]**

   When M=0, the circuit performs A+B

   When M=1, the circuit performs A-B

4. a) An 8×1 multiplexer has inputs A, B, and C connected to the selection inputs S_2, S_1, and S_0, respectively. The data inputs I_0 through I_7, are as follows: **[5]**

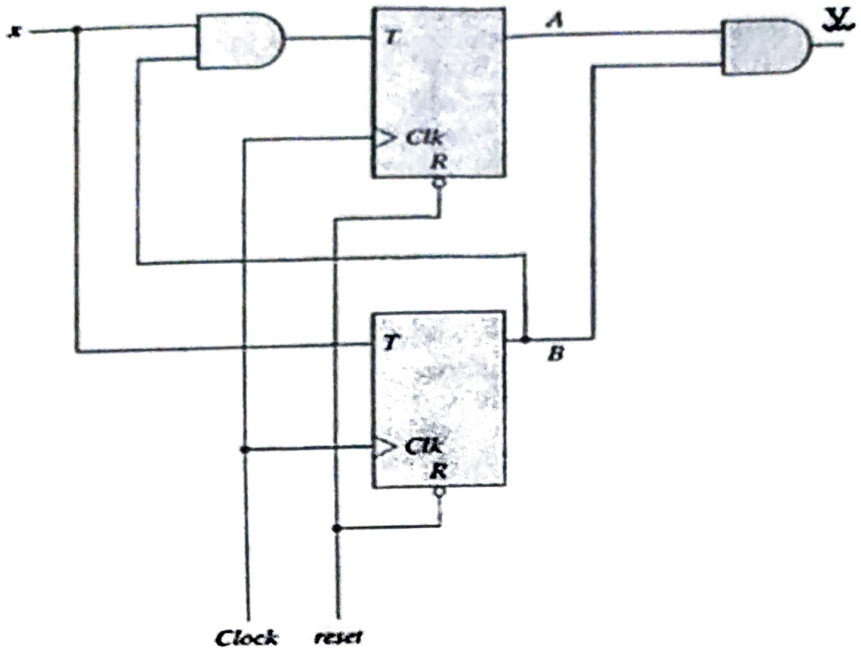
   $I_1=I_2=I_4=0$; $I_3=I_5=1$; $I_0=I_7=D$; and $I_6=D'$

   Determine the Boolean function that the multiplexer implements.

   b) Design 4 x 16 decoder using 2 x 4 decoders **[5]**

5. A bank has 3 locks with 1 key for each lock. Each key is owned by a different person. In order to open the vault atleast two people must insert their keys into the assigned locks. All the keys are not inserted at the same time. Write an equation for the variable Z which is 1 if and only if the door should open. Determine a truth table for the digital locking system. Design using k map techniques a minimum AND-OR gate network to realize this locking system.

6. Derive the state table and the state diagram of the sequential circuit shown in Figure and explain the function that the circuit performs.



7. Design a sequential circuit with two D flip flops A and B and one input x. When x = 0, the state of the circuit remains the same. When x = 1, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats.

8. a) Design a counter with the following repeated binary sequence 0, 1, 3, 7, 6, 4. [5]
Use T flip flops.

b) Construct an asynchronous Mod12 counter using JK flip flop. [5]

9. Construct a 5-bit serial in/serial out shift register using D flip flop. Apply the binary input 11010 into the register and sketch the waveform.

10. Draw a neat diagram of 8086 Architecture and explain the operation of the bus interface and execution unit in detail.

11. Write a 8086 assembly program to multiply two 8-bit numbers stored in P1 and P2 and store the result in P3, using both direct and indirect addressing mode.

12. With neat block diagram explain how 8255 Programmable Peripheral Interface is interfaced with 8086 microprocessor.

⇔⇔⇔ J/E/TX ⇔⇔⇔