



# VIT

Vellore Institute of Technology  
Vellore, Tamil Nadu, India

**SCHOOL OF ELECTRONICS ENGINEERING**  
**CONTINUOUS ASSESSMENT TEST - II**  
**FALL SEMESTER 2024-2025**

REG.NO.:

SLOT: E1+TE1

**Programme Name & Branch** : B.Tech -CSE

**Course Code and Course Name** : BECE102L & Digital Systems Design

**Faculty Name(s)** : Anitha R, Lavanya N, Palla Penchalaiah, Avinash Chandra, Rajesh N, Shweta B Thomas, Saurabh Nagar, Anju Thomas, Sidharth Gautam, Jaffino, Hemanta Kumar Sahu, Anand S, Nawaz Shafi, Vetriveeran Rajamani, Hemalatha K, Sukanta Kumar Tulo, Raja Sellappan, Niroj Kumar Sahu, Mangaiyarkarasi R

**Class Number(s)** : VL2024250104311, VL2024250104284, VL2024250104278, VL2024250104266, VL2024250104273, VL2024250104287, VL2024250104292, VL2024250104293, VL2024250104269, VL2024250104256, VL2024250104299, VL2024250104264, VL2024250104297, VL2024250104262, VL2024250104310, VL2024250104276, VL2024250104271, VL2024250104252

**Date of Examination** : 17-Oct-2024

**Exam Duration** : 90 minutes

**Maximum Marks: 50**

**General instruction(s):**

- Answer All Questions

**Questions**

1. Design a Priority Encoder which has 4 inputs, the case in which the priority order is  $D2 > D0 > D3 > D1$  (D2 is the highest Priority and D1 is the Lowest priority). Write the Verilog code for the same using behaviour level modelling. 10
2. Assume that registers M and Q of the sequential Booth's multiplier are initialized with the values - 15 and 7. 10
  - 1) Perform the multiplication operation according to Booth's algorithm.
  - 2) After multiplication, how many subtraction and addition operations will be performed? Write the answer in decimal.
3. Obtain the Boolean expressions ( $A > B$ ,  $A = B$  and  $A < B$ ) for 3-bit magnitude comparator. Based on the comparison, develop a control network to perform the following operation in block diagram level. 10
  - a. If  $A = B$ , Perform binary addition
  - b. If  $A > B$ , Perform array multiplication
  - c. If  $A < B$ , Perform two complement subtraction



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4. A M-F flip-flop behaves as follows:
- If MF = 01, the flip-flop changes state.
  - If MF = 11, the flip-flop is set to Q = 0.
  - If MF = 00, the flip-flop is set to Q = 1.
  - The input combination MF = 10 is not allowed.
- (a) Give the characteristic (next-state) equation for this flip-flop.  
 (b) Complete the table, using don't-cares where possible.

Q	Q <sup>+</sup>	M	F
0	0		
0	1		
1	0		
1	1		

- (c) Realize the following next-state equation for Q using a MF flip-flop:

$$Q^+ = CQ + D\bar{Q}. \text{ Find equations for M and F.}$$

5. Using positive edge triggering SR flip flop, design a synchronous counter which counts the following sequence
- 000, 111, 110, 101, 100, 011, 010, 001, 000

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