VIT
Vellore Institute of Technology

School of Computer Science and Engineering

Fall Semester 2022-2023

Continuous Assessment Test – II

Programme Name & Branch : BTECH CSE **SLOT: D1+TD1**

Course Name & code: Digital Systems Design BECE102L

Class Number (s): VL2022230104429, VL2022230104434, VL2022230104441, VL2022230104438, VL2022230104437, VL2022230104441, VL2022230104447, VL2022230104445, VL2022230104452, VL2022230104574

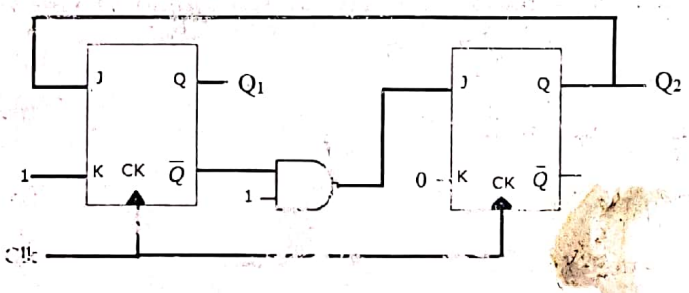
Faculty Name (s): JAYAKRISHNAN P, SHWETA B THOMAS, MANGAIYARKARASI R, DEBASHIS MAJI, SUMIT KUMAR JINDAL, RAJESH G, DEBASHISH DASH, ANJU THOMAS, VIKAS VIJAYVARGIYA, KUMARANARAYANA SWAMY C, DINAH ANN VARUGHESE

Exam Duration: 90 Min. **Maximum Marks: 50**

General instruction(s):

Mention the question number outside the margin clearly. Answer in sequential order with clarity. Draw the diagrams neatly using appropriate pencil and scale.

Q.No.	Questions	Max Marks
1.	i. Implement the following Boolean function using a multiplexer. $F(A,B,C,D) = \sum(0,1,5,6,9,11,12,13,14)$ ii. For the above design, write a verilog code using conditional operator.	5 5
2.	Implement a 2-bit magnitude comparator using 4to16 decoder	10
3.	i. Consider a data transmission system used to transmit 4-bit data. The system uses odd parity to detect the error in transmission. Design a system that generates the parity bit at the transmitter side and checks the parity at receiver side. ii. Write a Verilog code for the above design.	5 5

4.	i. Design a D-Flip flop using T Flip Flop ii. Write a verilog code for the above design using structural modelling.	5 5
5.	In the sequential circuit using JK Flip Flop given below, assume that the initial value of $Q_1 = 0$ & $Q_2 = 1$ and give the function table and draw the wave sequences of the outputs Q_1 and Q_2 for 6 positive edge clock cycles. 	10

$(A=B) = D_0 + D_5 + D_{10} + D_{15}$

$(A>B) = D_4 + D_8 + D_9 + D_{12} + D_{13} + D_{14}$

$(A<B) = D_1 + D_2 + D_3 + D_6 + D_7 + D_{11}$