Vellore – 632014, Tamil Nadu, India

SCHOOL OF ELECTRICAL ENGINEERING

FALL SEMESTER 2023-2024

CAT-II

SLOT: D1

Programme Name & Branch : B.Tech (EEE & EIE) Course Code: BEEE205L

Course Name : Electronic Devices & Circuits

Faculty Members : Dr. M.N. Venkataraman, Dr. P. Uma Sathyakam, Dr. R. Gnanavignesh

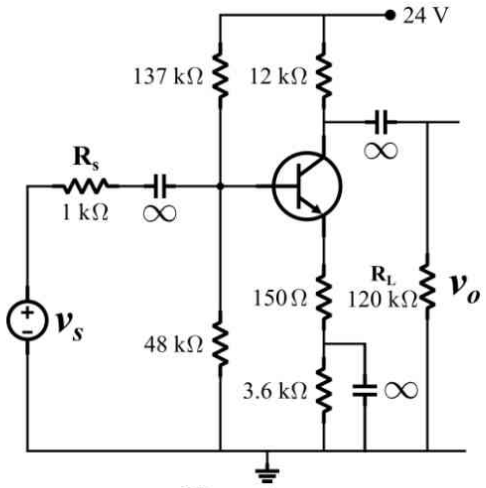
Class Number(s) : VL2023240103145

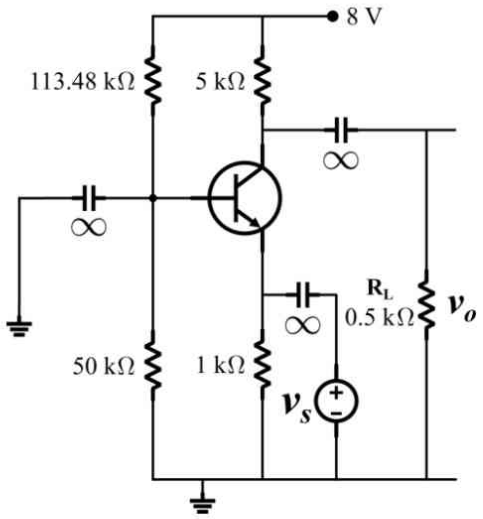
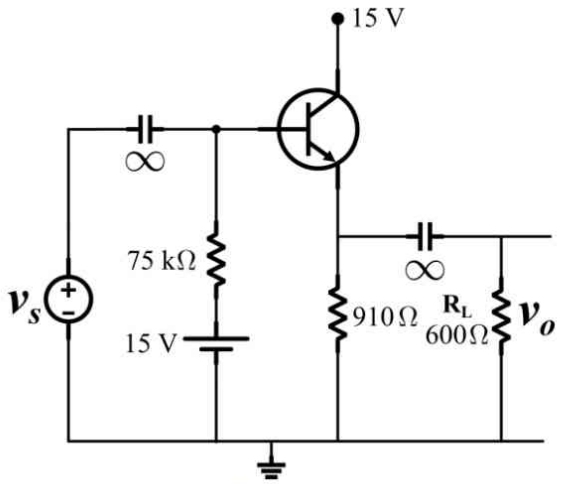
Date of the Examination : 18-October-2023

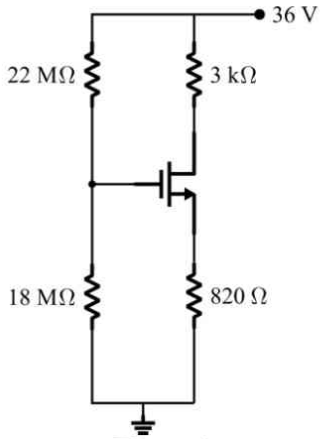
Duration : 90 minutes **Max. Marks : 50**

General instruction(s): ***Use calculator to the numerical with three decimal points.***

Answer ALL Questions

Q. No.	Question	Max. Marks	CO	BL
1.	Figure 1 depicts a partially bypassed common emitter amplifier. Find the following metrics for the amplifier if $\beta = 100$ and $V_{BE,ON} = 0.7$ V. a) DC operating conditions (2.5 marks) b) Input impedance (2.5 marks) c) Overall voltage gain (2.5 marks) d) Output impedance (2.5 marks)  **Figure 1**	10	2	L3

2.	For the amplifier depicted in Figure 2, the input signal source v_s is a sinusoid of frequency 50 Hz and amplitude of 5 mV. The output load is denoted by R_L. With the given parameters $\alpha = 0.98$ and $V_{BE,ON} = 0.7$ V, determine the following a) Input impedance (2.5 marks) b) Overall voltage gain (2.5 marks) c) Output impedance (2.5 marks) d) Output voltage amplitude in mV (2.5 marks)  Figure 2	10	2	L4
3.	For the emitter follower shown in Figure 3, $\beta = 100$ and $V_{BE,ON} = 0.7$ V. Obtain the following: a) Input impedance (2 marks) b) Voltage gain (2 marks) c) Output impedance (3 marks) d) Proof that the device small signal voltage gain is always less than 1. (3 marks)  Figure 3	10	2	L5

4.	Explain with appropriate diagrams, the working principle of a n-channel enhancement MOSFET.	10	2	L2
5.	Find V_{GS}, I_D and V_{DS} for the following circuit shown in Figure 4. The given parameters for the n-channel enhancement MOSFET are V_{TN} = 5 V, K = 0.12 mA/V^2.  Figure 4	10	2	L5

Question Paper Setter: Dr. R. Gnanavignesh

Moderator: Dr. Vidhyasagar